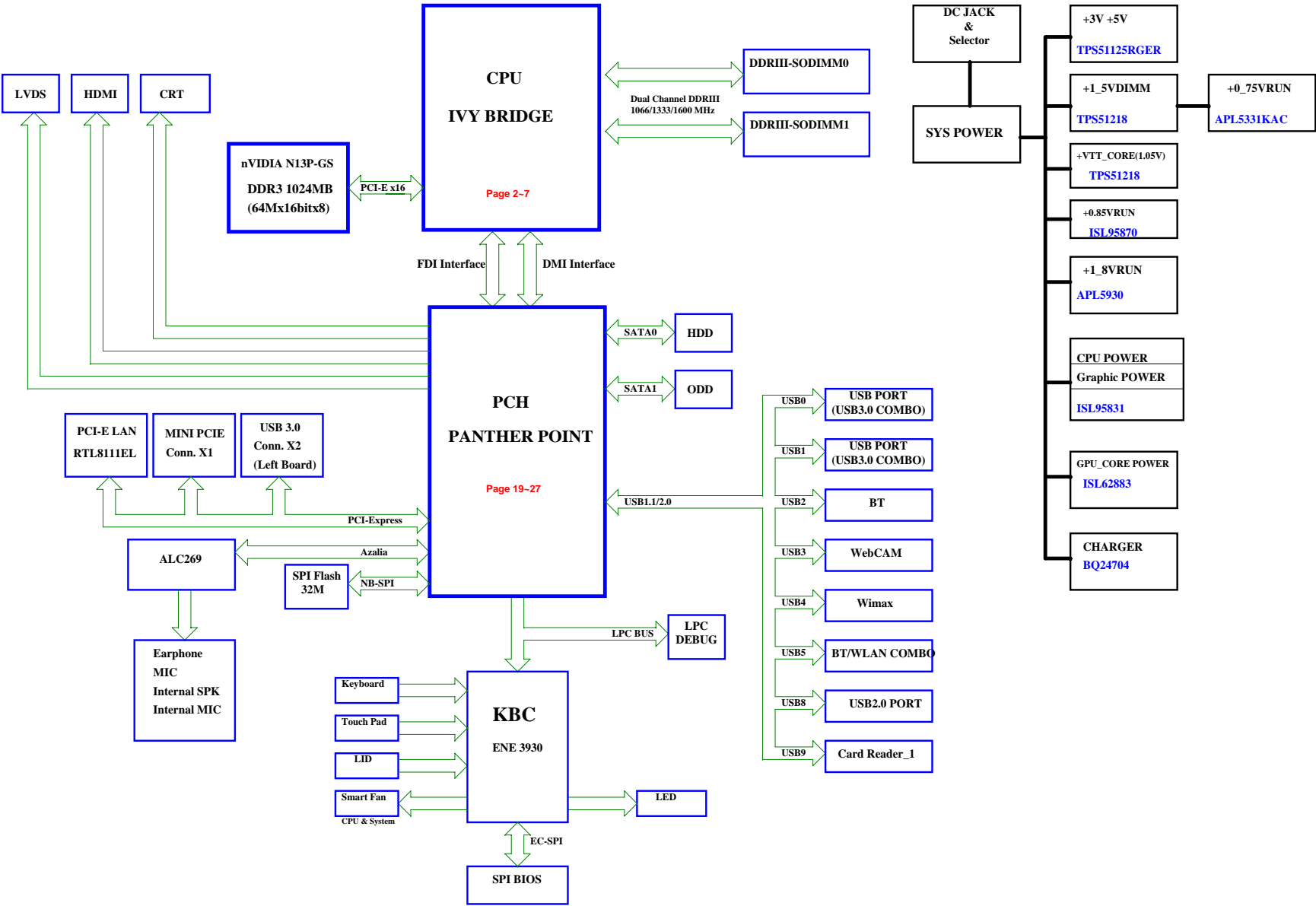


MS-16GB Ver : 0A (nVIDIA N13P-GS/GL)

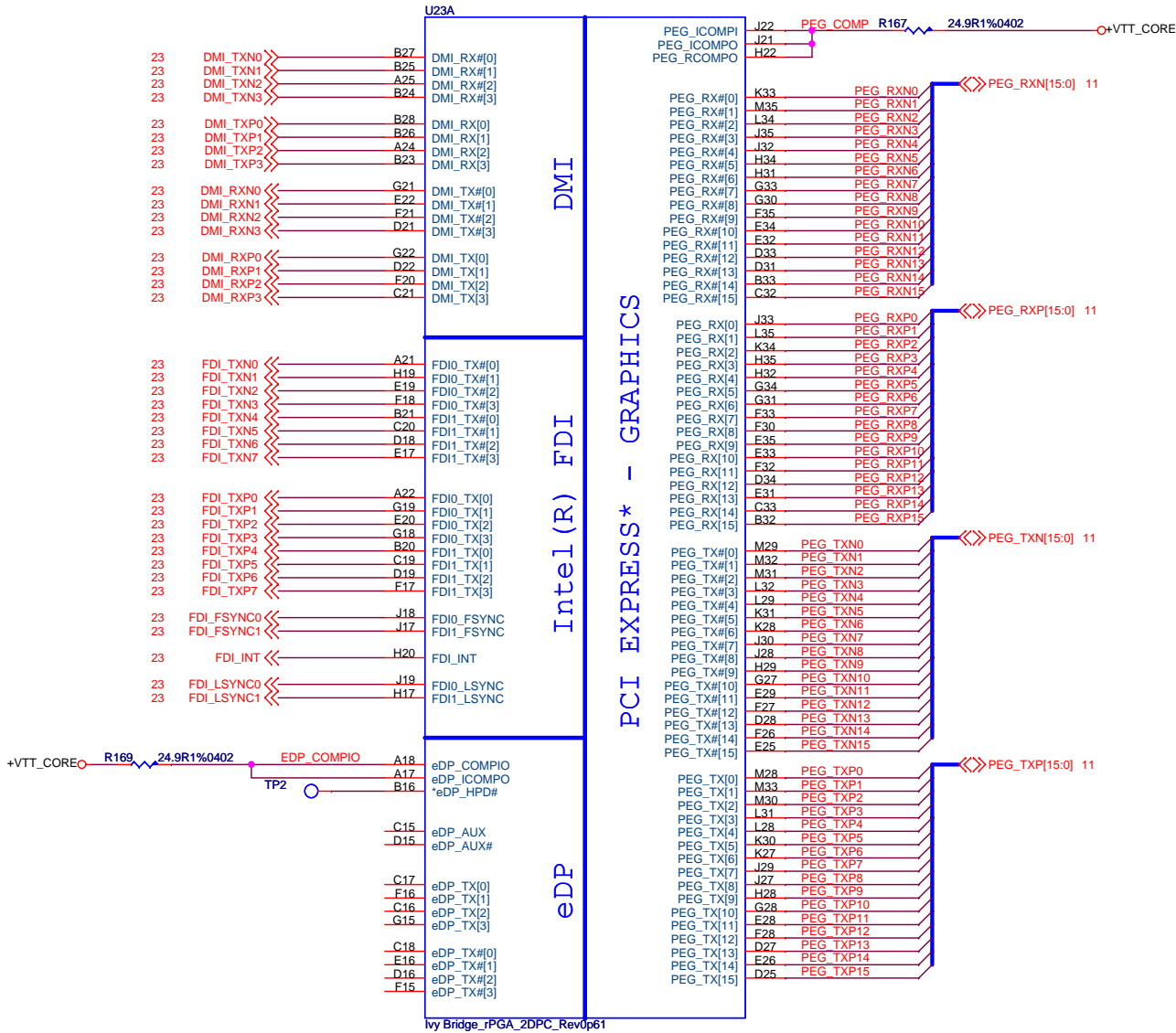
Chief River Platform

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09	DDR3 SODIMM 1
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11	nVIDIA N12P-GS_MEM Interface A
12	nVIDIA N12P-GS_MEM Interface C
13	nVIDIA N12P-GS_FrameA DDR3 I
14	nVIDIA N12P-GS_FrameA DDR3 II
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26	PCH-7 (POWER)
27	PCH-8 (POWER)
28	PCH-9 (GND)
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34	Battery Select & Charger
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36	M_SMDDR_VTERM /I_5VRUN
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38	M_0.85VRUN & 1.8VRUN
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41	Screw / ME
42	EMI
43	[A] CRT/USB/LAN/BT/CONN
44	[A] PCIe GLAN(RTL 8111E)
45	[B] AUDIO/CONN
46	[B] USB3.0
47	[C] PWR_SW /LED Launch Board



IVY BRIDGE PROCESSOR (HOST)



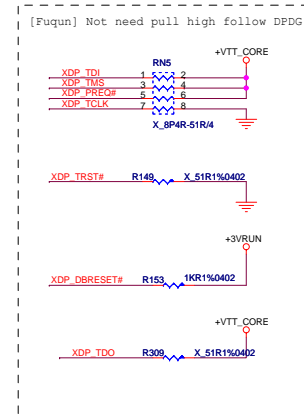
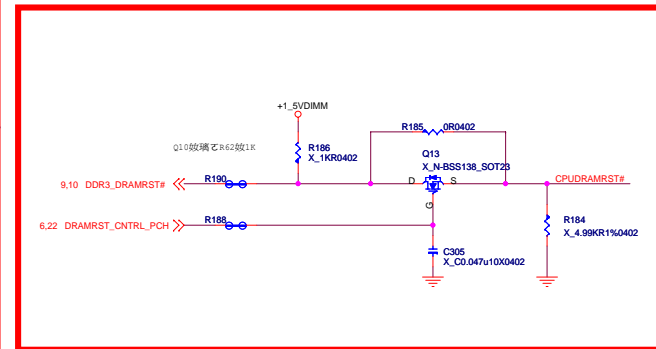
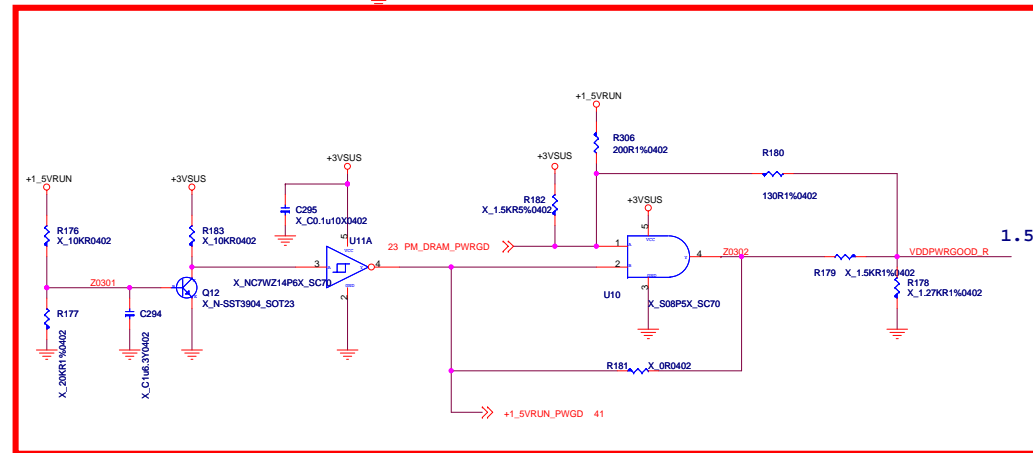
Title		
PROCESSOR-1 (HOST BUS)		
Size	Document Number	Rev
B	MS-16GB	1.0
Date:	Tuesday, January 03, 2012	Sheet 2 of 56

IVY BRIDGE PROCESSOR (CLK, MISC, JTAG)

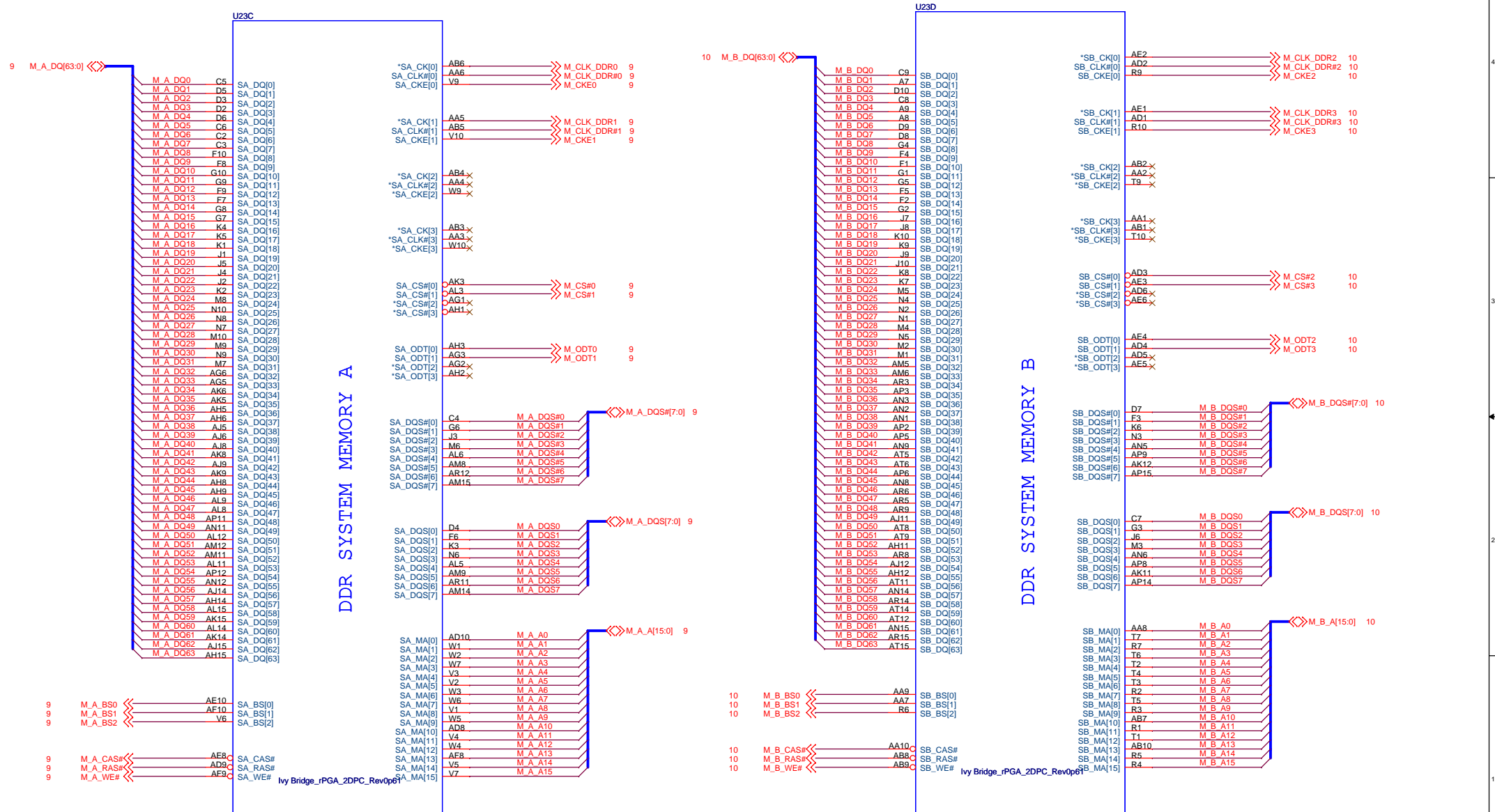
If use EC_PROCHOT#, R310 need staff, R148 need change to 62ohm, R158 need change to 56ohm;

PLT_RST#_R set lv level: R334 1.5K, R3370 649R;
PLT_RST#_R set 1.05v level: R334 1.47K, R3370 681R;

[Fuqun] Follow MS-16F3



IVY BRIDGE PROCESSOR (DDR3)



IVY BRIDGE PROCESSOR (POWER)

[Fugun] 0.3-1.52V
[Fugun] 45W----94A
35W----52A

POWER

[Fugun] 22u*16/10u*10

52 A

8.5 A

1.05V

CORE SUPPLY

SVID

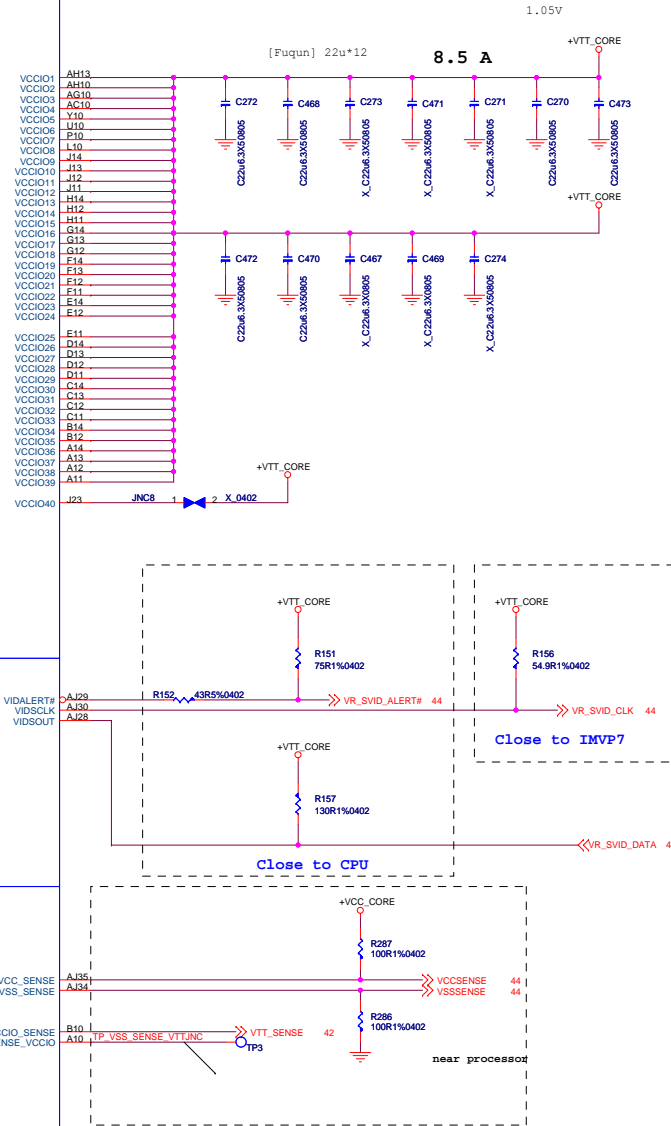
SENSE LINES

PEG AND DDR

Ivy Bridge_PGA_RDPD_Rev0p61

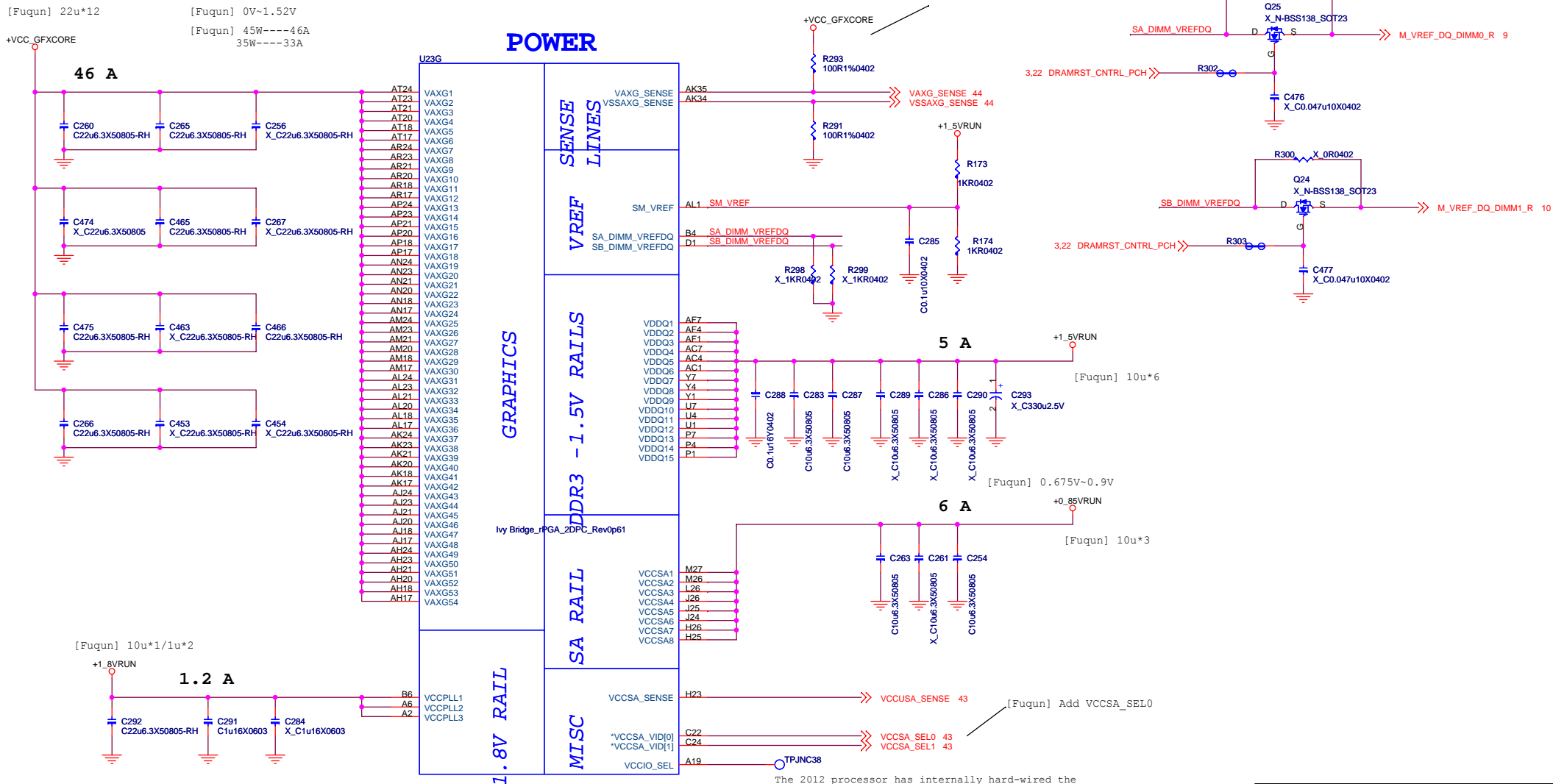
VIDALERT#
VIDCLK
VIDOUT

VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSS_SENSE_VCCIO



IVY BRIDGE PROCESSOR (GRAPHICS POWER)

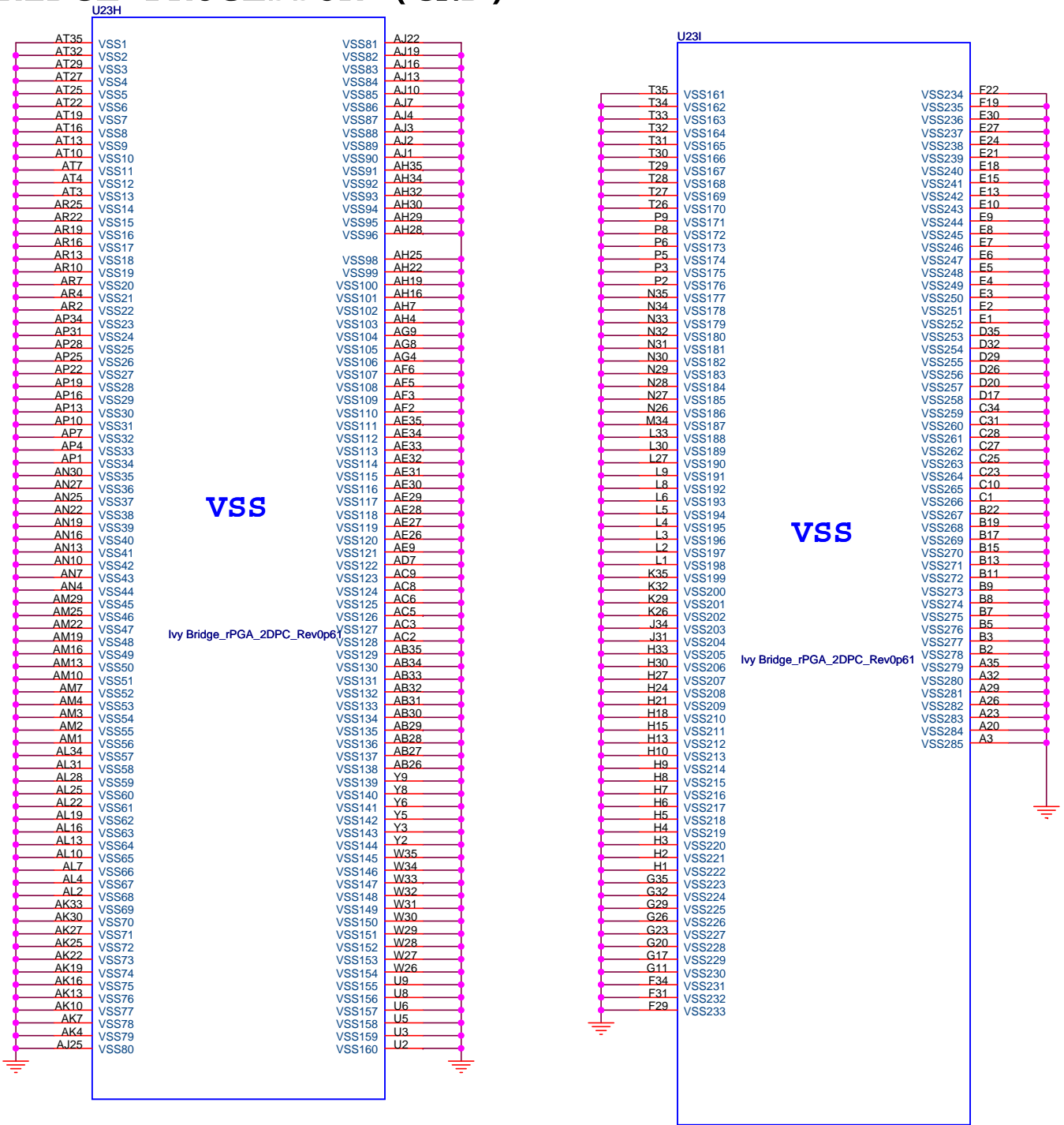
PPDG Recommend 100R



The 2012 processor has internally hard-wired the VCCIO_SEL pin low, so removal of this series resistor will restore the signal to the *1\$ level for a 1.05-V selection.

Title			
PROCESSOR-5 (GRAPHICS POWER)			
Size	Document Number	Rev	
Custom	MS-16GB	1.0	
Date:	Tuesday, January 03, 2012	Sheet	6 of 56

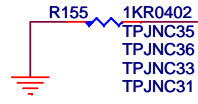
IVY BRIDGE PROCESSOR (GND)



Title				
PROCESSOR-6 (GND)				
Size	Document Number			Rev
Custom	MS-16GB			
Date:	Tuesday, January 03, 2012	Sheet	7 of 56	1.0

IVY BRIDGE PROCESSOR (RESERVED)

UMA: NC R155



TPJNC64
TPJNC32
TPJNC63
TPJNC28

AK28
AK29
AL26
AL27
AK26
AL29
AL30
AM31
AM32
AM30
AM28
AM26
AN28
AN31
AN26
AM27
AK31
AN29
AJ31
AH31
AJ33
AH33
AJ26
F25
F24
F23
D24
G25
G24
E23
D23
C30
A31
B30
B29
D30
B31
A30
C29
J20
B18
J15

U23E

CFG[0]
CFG[1]
CFG[2]
CFG[3]
CFG[4]
CFG[5]
CFG[6]
CFG[7]
CFG[8]
CFG[9]
CFG[10]
CFG[11]
CFG[12]
CFG[13]
CFG[14]
CFG[15]
CFG[16]
CFG[17]

VAXG_VAL_SENSE
VSSAXG_VAL_SENSE
VCC_VAL_SENSE
VSS_VAL_SENSE

RSVD5

RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
RSVD21
RSVD22
RSVD23

RSVD24
RSVD25

RSVD27

*VCC_DIE_SENSE
*VSS_DIE_SENSE

RSVD28
RSVD29
RSVD30
RSVD31
RSVD32

RSVD33
RSVD34
RSVD35

RSVD37
RSVD38
RSVD39
RSVD40

*RSVD_NCTF1
*RSVD_NCTF2
*RSVD_NCTF3
*RSVD_NCTF4
*RSVD_NCTF5

*RSVD_NCTF6
*RSVD_NCTF7
*RSVD_NCTF8
*RSVD_NCTF9
*RSVD_NCTF10

RSVD51
RSVD52

*BCLK_ITP
*BCLK_ITP#

*RSVD_NCTF11
*RSVD_NCTF12
*RSVD_NCTF13

KEY

AH27
AH26

L7
AG7
AE7
AK2
W8

AT26
AM33
AJ27

T8
J16
H16
G16

AR35
AT34
AT33
AP35
AR34

B34
A33
A34
B35
C35

AJ32
AK32

AN35
AM35

AT2
AT1
AR1

B1

TPJNC34
TPJNC37
TPJNC39
TPJNC41
TPJNC40
TPJNC43

these PINs for debug purpose

CFG2 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

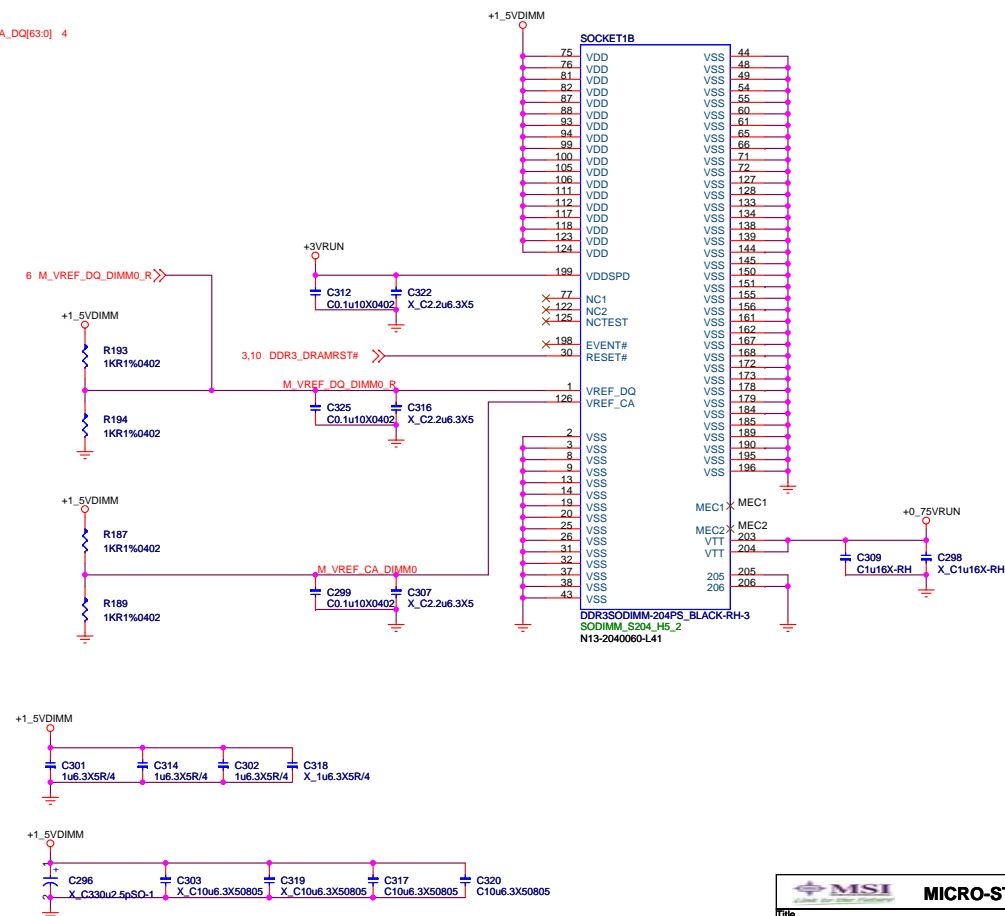
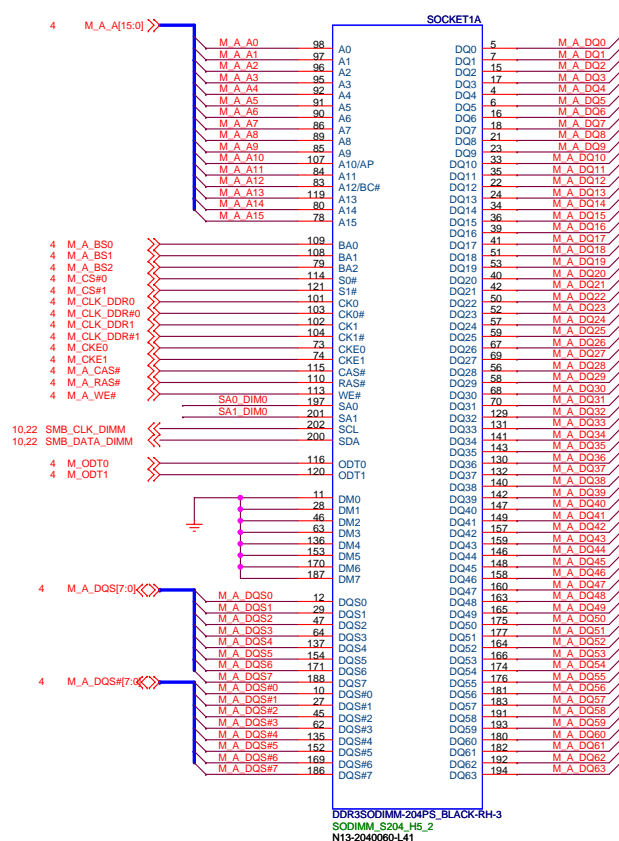
PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

Ivy Bridge_rPGA_2DPC_Rev0p61

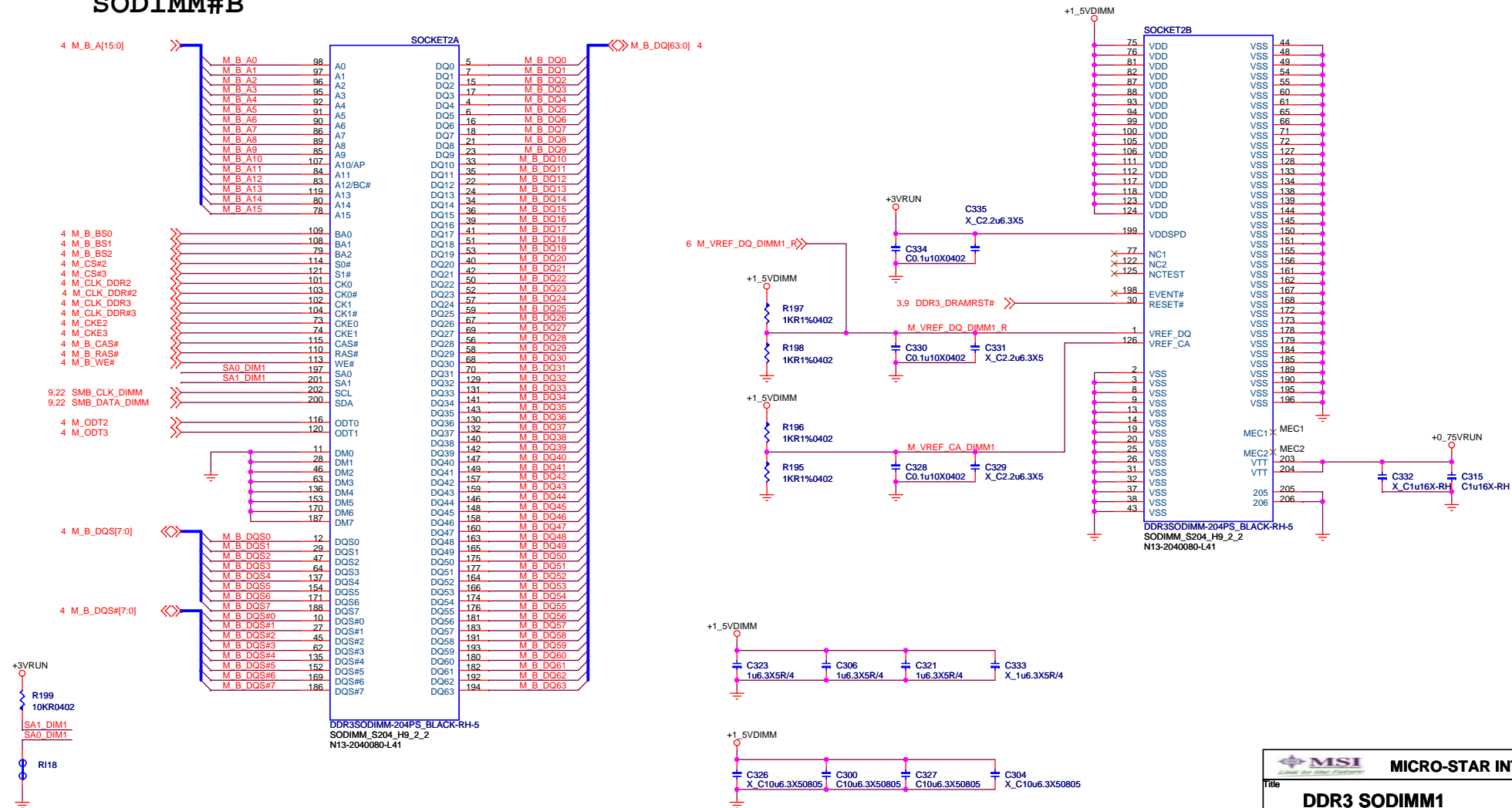
RESERVED

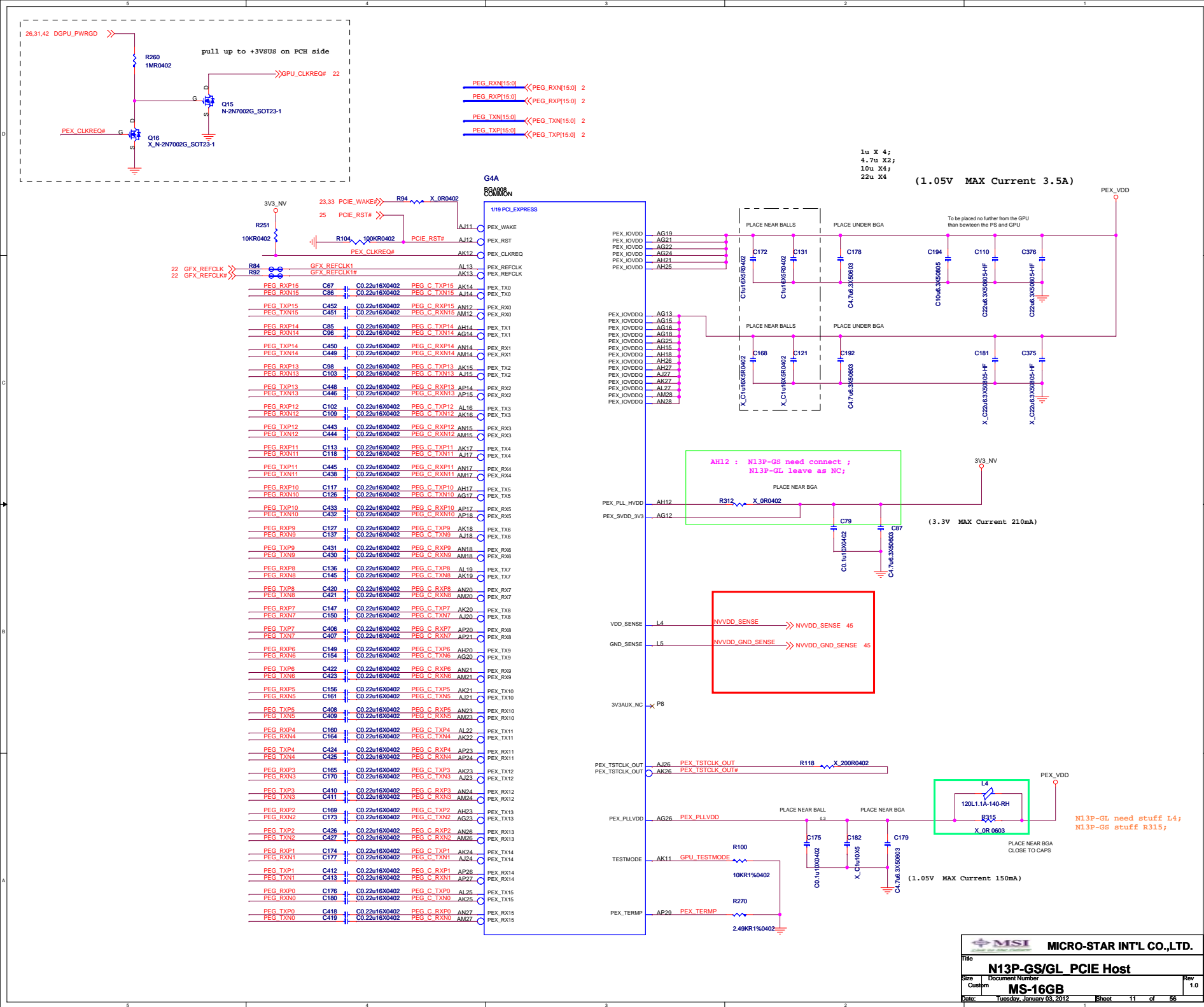
PROCESSOR-7 (RESERVE)		
Size	Document Number	Rev
Custom	MS-16GB	1.0
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SODIMM#A



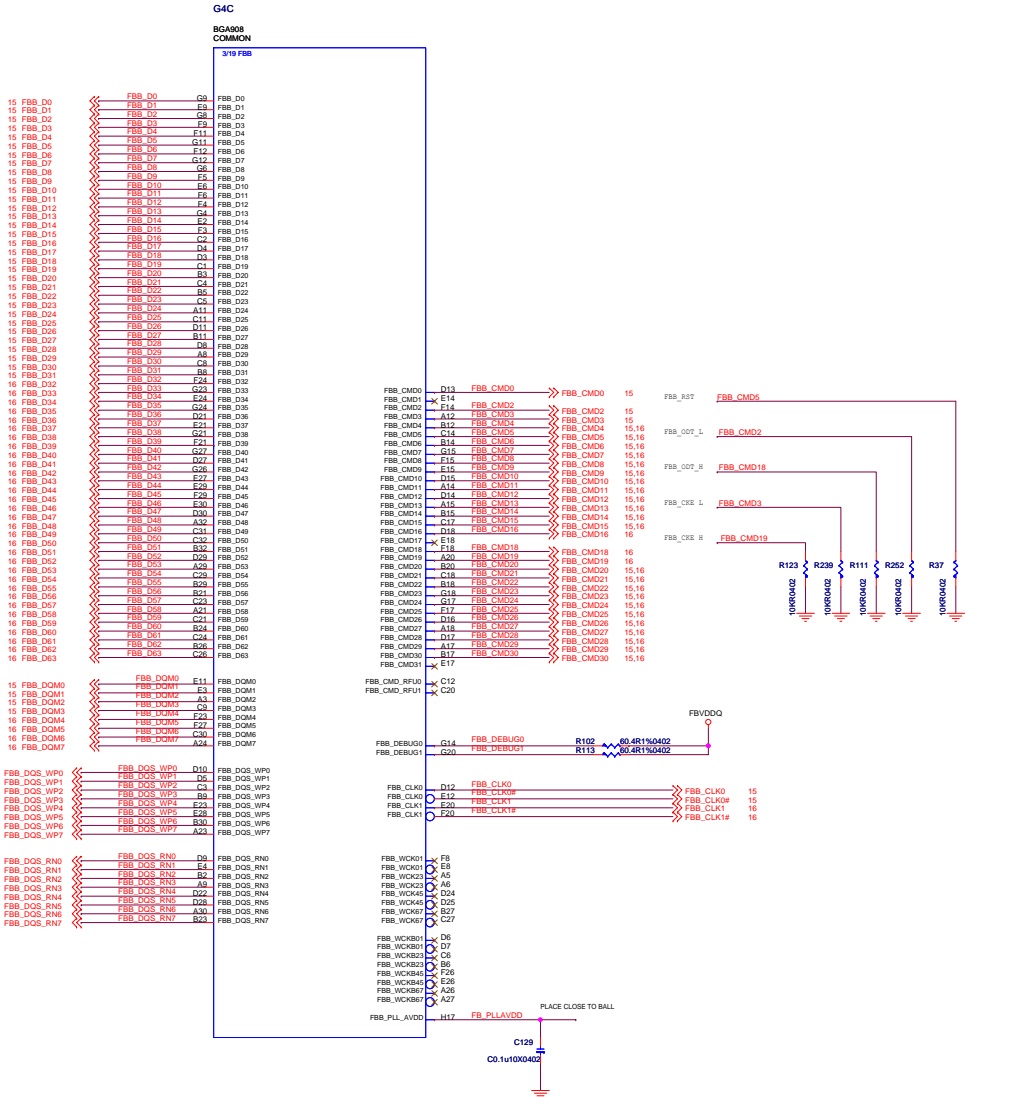
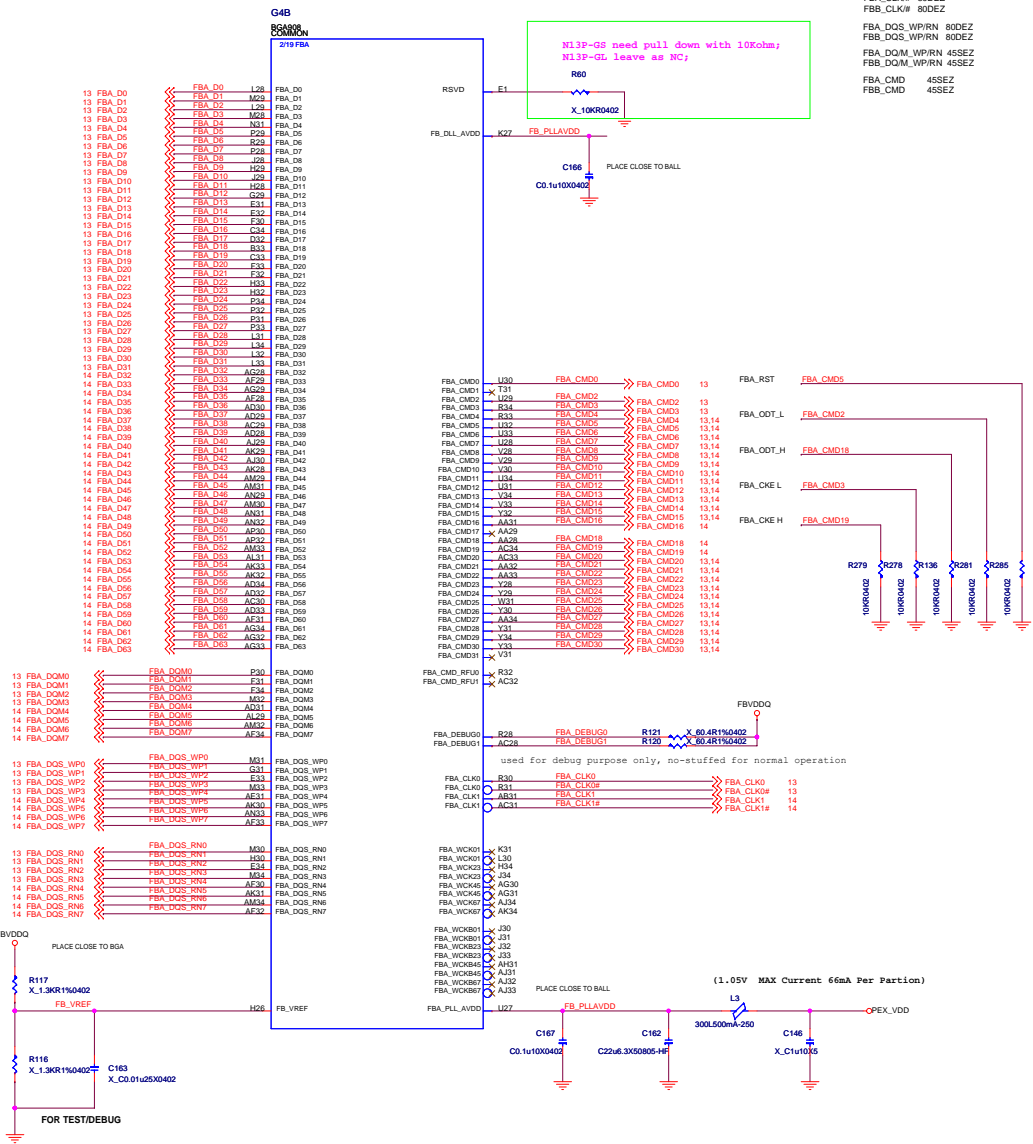
SODIMM#B



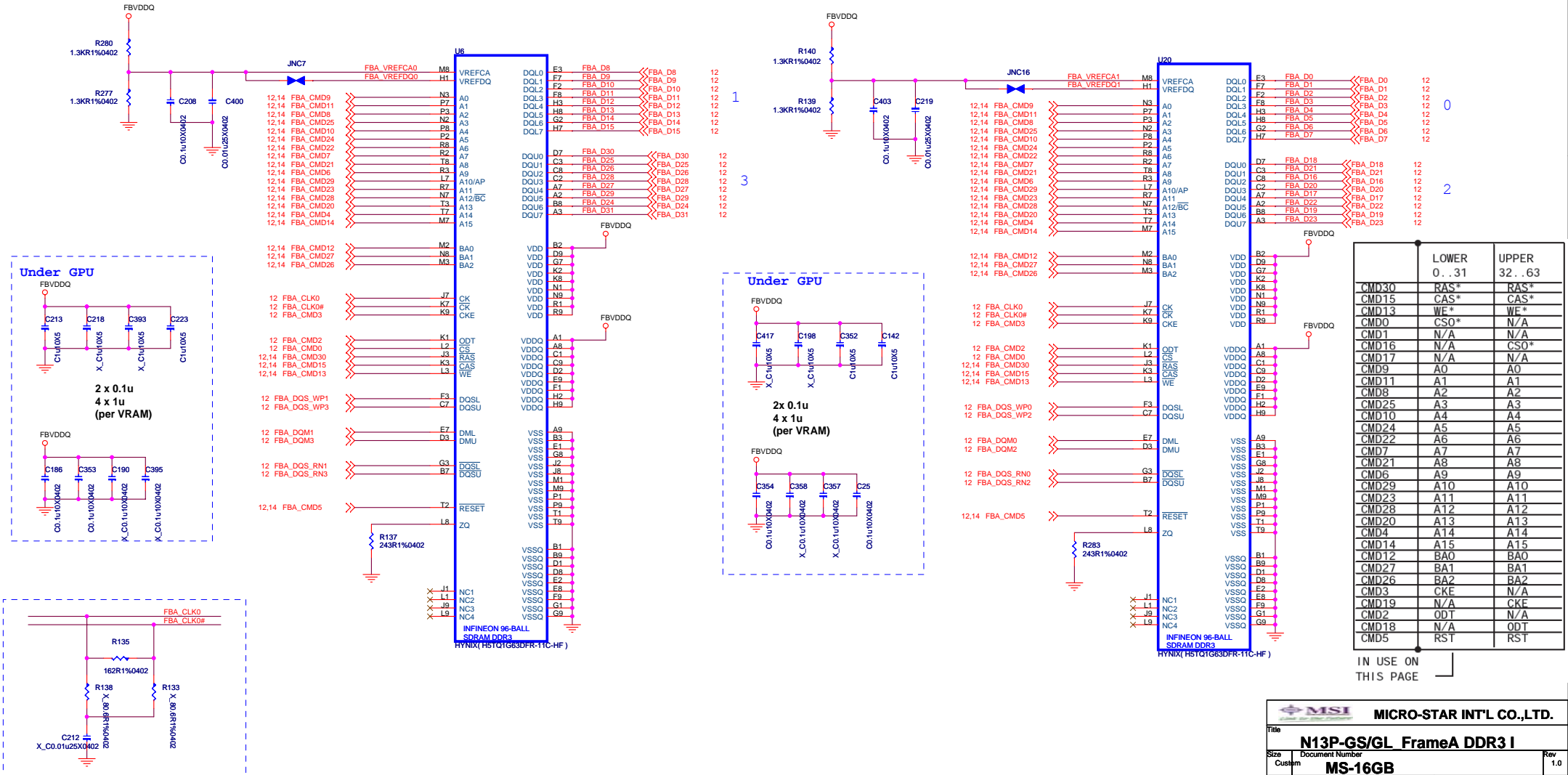


Frame Buffer Partitions A/B

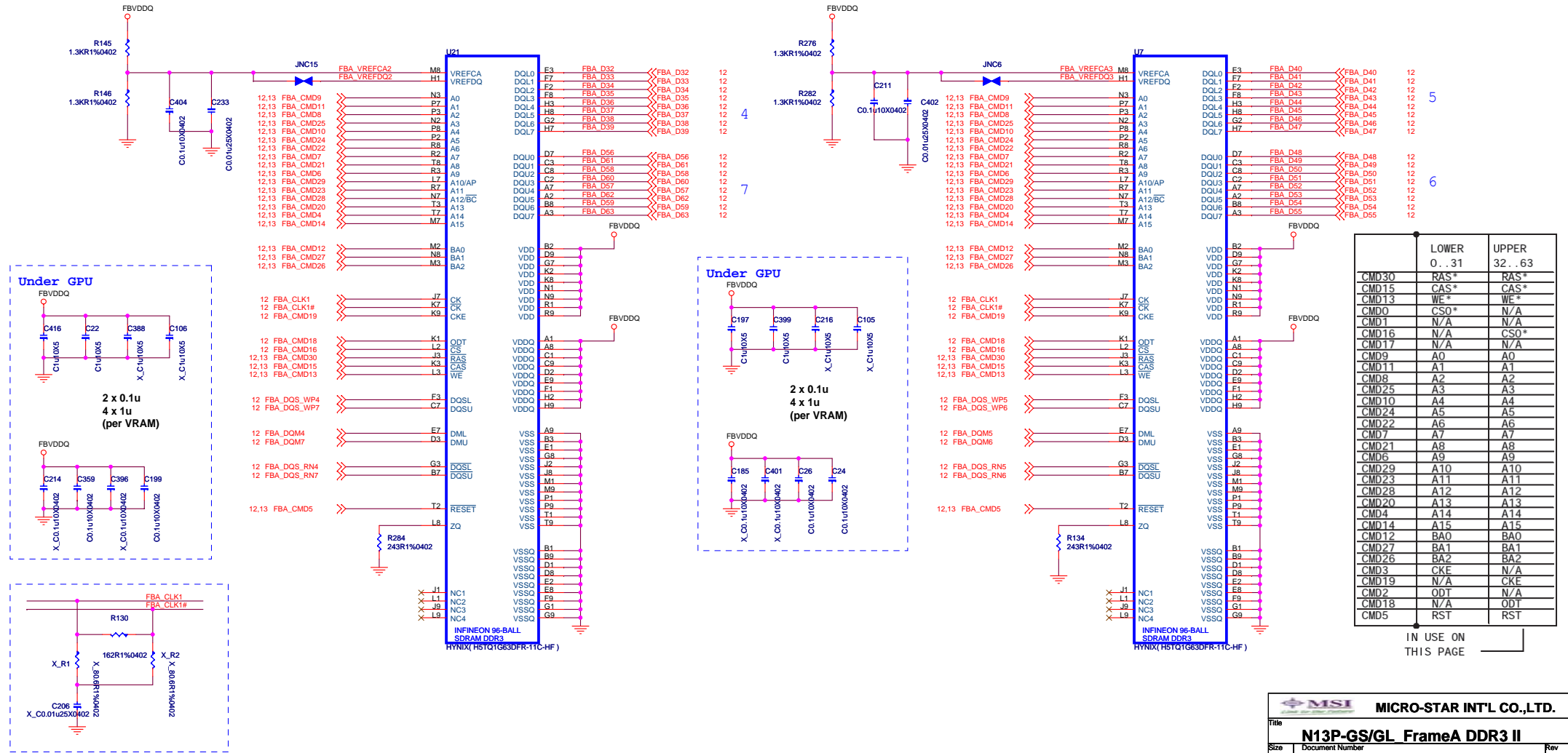
impedance???



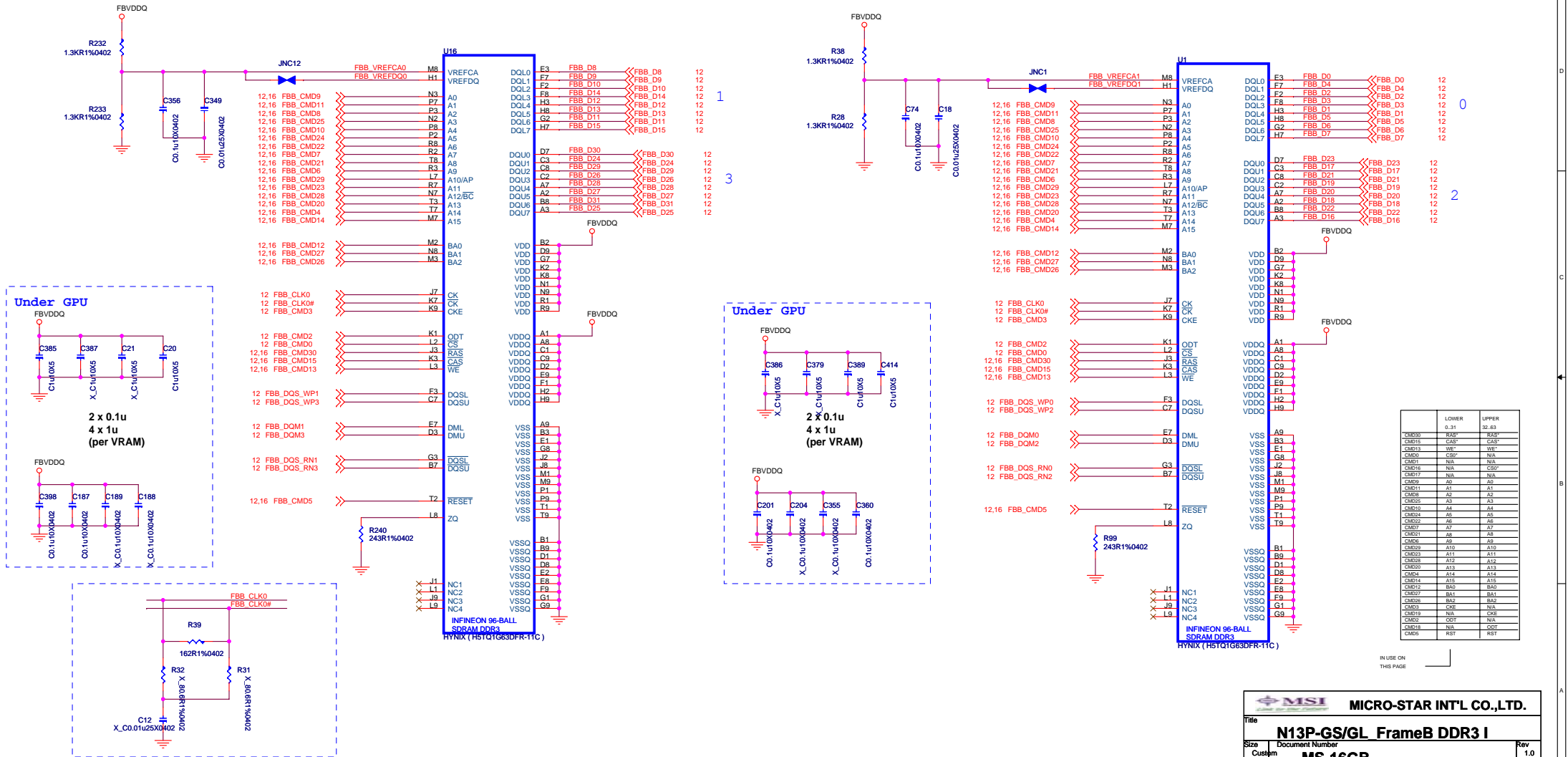
Memory Lower Partition A



Memory Upper Partition A



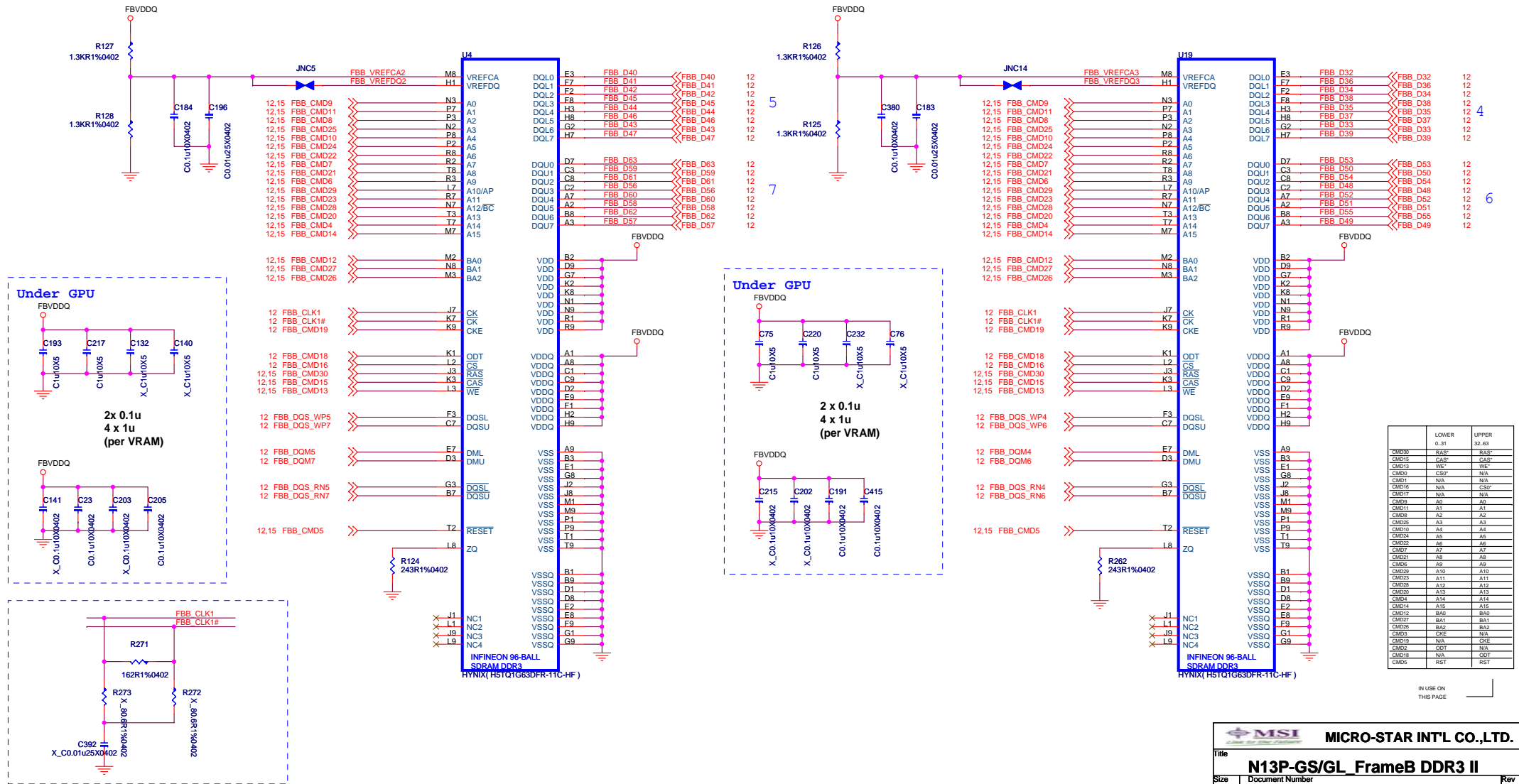
Memory Lower Partition B



IN USE ON
THIS PAGE

MICRO-STAR INT'L CO.,LTD.	
Title N13P-GS/GL FrameB DDR3 I	
Size Custom	Document Number MS-16GB
Date: Tuesday, January 03, 2012	Sheet 15 of 56
Rev 1.0	

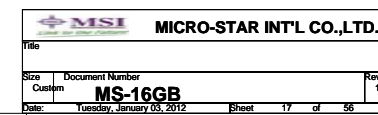
Memory Upper Partition B



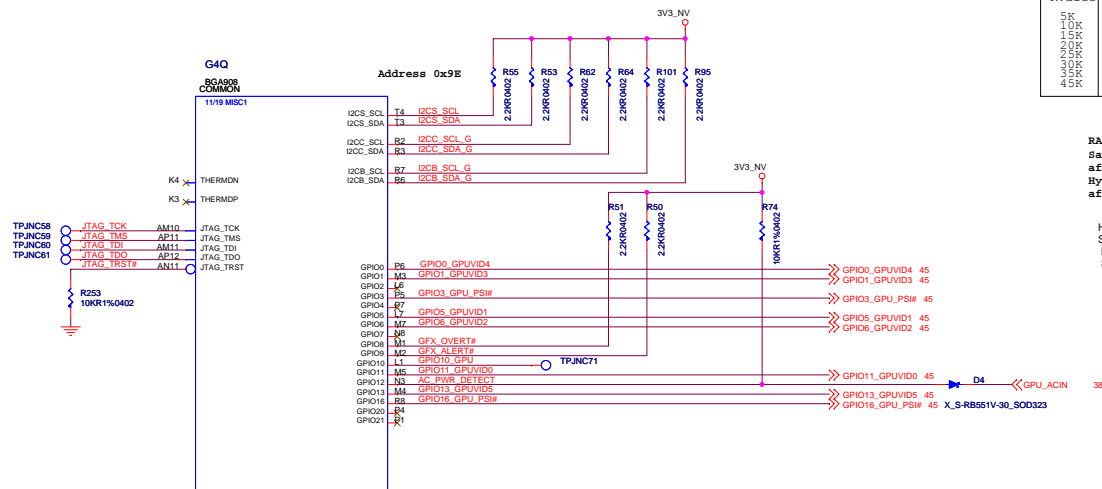
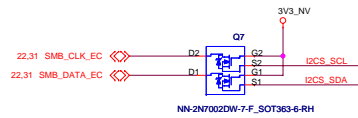
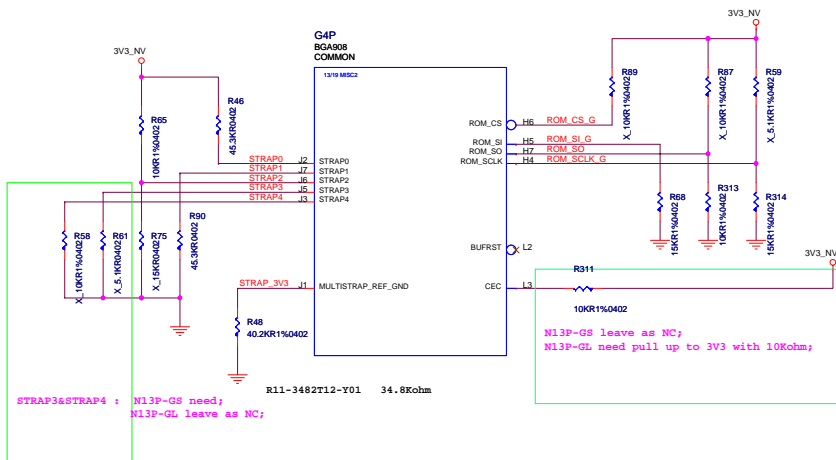
	LOWER	UPPER
	0.31	32.63
CM006	RAS*	RAS*
CM016	CAS*	CAS*
CM013	WE*	WE*
CM018	CSF*	CSF*
CM011	N/A	N/A
CM016	N/A	CSF*
CM017	N/A	N/A
CM009	A0	A0
CM011	A1	A1
CM010	A2	A2
CM025	A3	A3
CM010	A4	A4
CM020	A5	A5
CM021	A6	A6
CM007	A7	A7
CM021	A8	A8
CM008	A9	A9
CM020	A10	A10
CM023	A11	A11
CM022	A12	A12
CM020	A13	A13
CM004	A14	A14
CM021	A15	A15
CM012	BA0	BA0
CM027	BA1	BA1
CM026	BA2	BA2
CM003	CXE	N/A
CM019	N/A	CXE
CM02	CDT	CDT
CM005	ODT	RST

IN USE ON
THIS PAGE

G4J



GPIOs, Thermal Sensor, I2C/GPIO Expanders

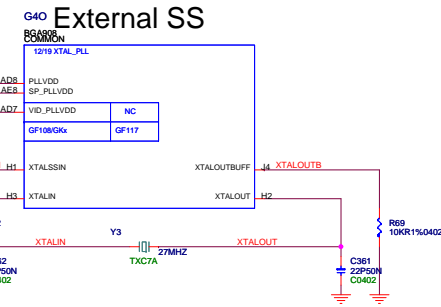


Item	N13P-G5	N13P-GL
Device ID	0x0FD2	0x0DE9
Package	GB4-128	GB4-128
Internal P/N	GK107, 28nm	GF108, 40nm
ROM_Si	Hynix 64x16, 15k pull down	Hynix 64x16, 15k pull down
	Samsung 64x16, 20k pull down	Samsung 64x16, 20k pull down
	Hynix 128x16, 35k pull down	Hynix 128x16, 35k pull down
	Samsung 128x16, 45k pull down	Samsung 128x16, 45k pull down
ROM_SO	0x9, 10k pull high	10k pull low
ROM_SCL	0x8, 5k PU	15k pull low
Strap0	0xF, 45k pull up	45k pull up
Strap1	0x6, 35k pull down	45k pull down
Strap2	15k pull down	10k pull up
Strap3	5k pull down	NC
Strap4	30k pull low	NC
NVDD Boot Voltage	0.9V	0.95V

Rvalue	Pull up	Pull down
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

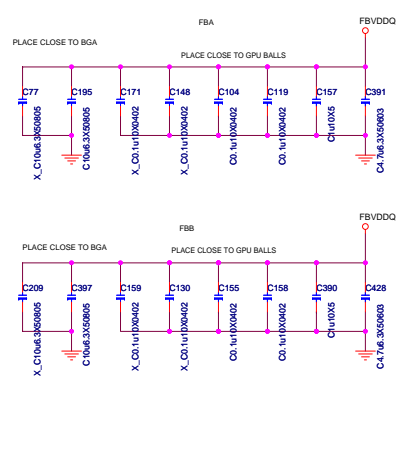
```
RAM CFG:
Samsung strap 0x3, K4W1G1646G-BC11
after date code 1113;
Hynix strap 0x2, H5TQ1G63DFR- 11C
after date code 1104
```

Hynix 64Mx16-----PD15K;
Samsung 64Mx16----PD20K
Hynix 128Mx16-----PD35K;
Samsung 128Mx16----PD45K

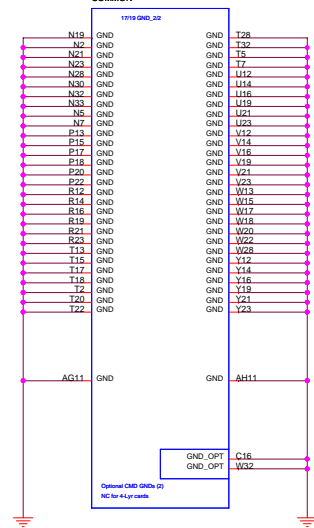
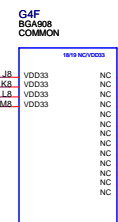
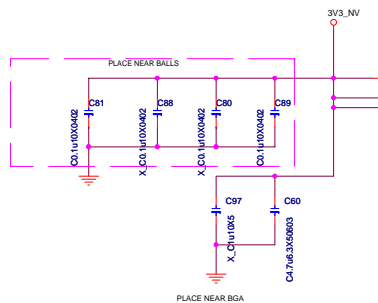
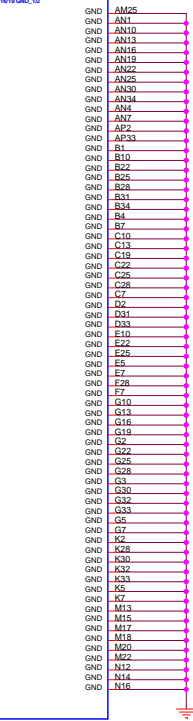
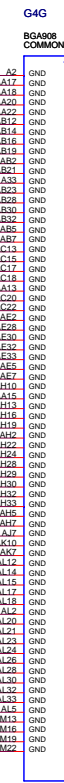
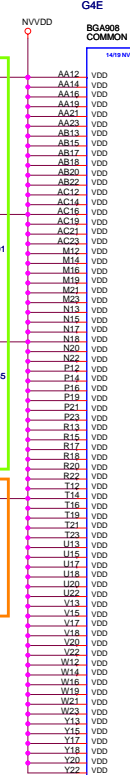
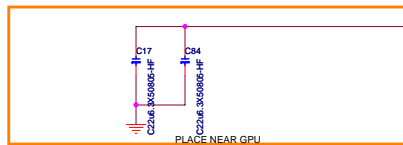
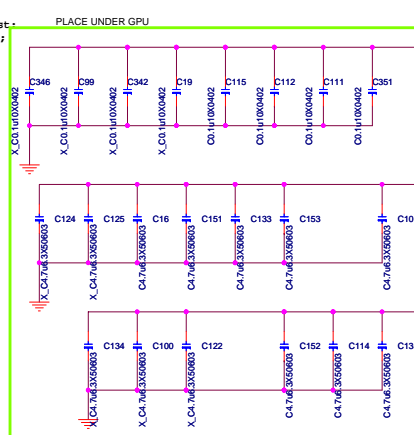
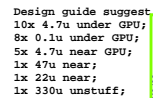
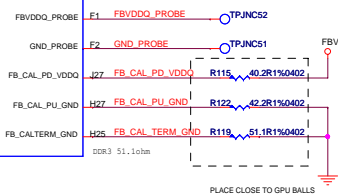
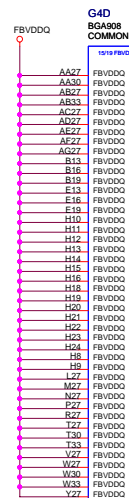


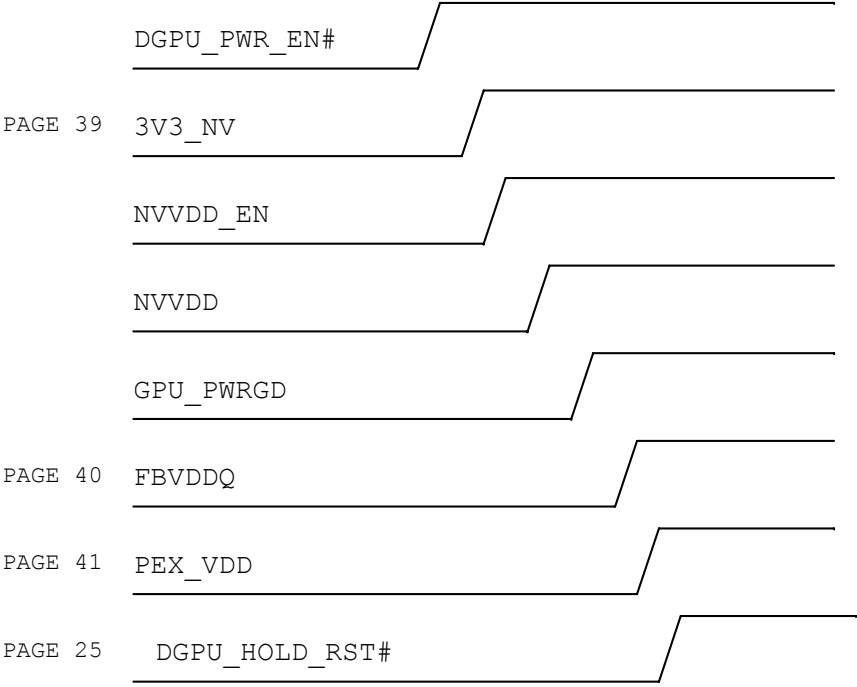
Strap Pin	strapping bit3	strapping bit2	strapping bit1	strapping bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	1	0 no video bios ROM	0	0
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
	0	0	1	0 (1)
ROM_SO	FB[1] 1 (0) FB Aperture size 256MB Default	FB[0]	SMR_ALT_LAYER 0 not multi-GPU usage	VGA_DEVICE 1 VGA device
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3G0_PAD_CFG_ADR[3]	3G10_PAD_CFG_ADR[2]	3G10_PAD_CFG_ADR[1]	3G10_PAD_CFG_ADR[0]
	0	1	1	0
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	0	0	1	0
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	0	0	0	0
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	0 (1)	0	1	1

Power/Decoupling: NVVDD, 3V3_NV, GRND, and Optional



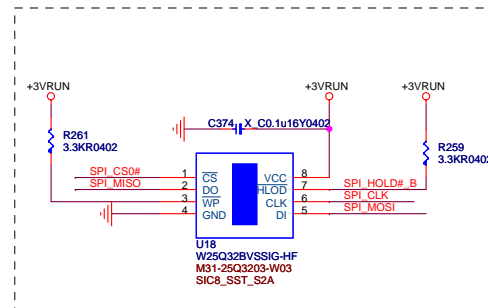
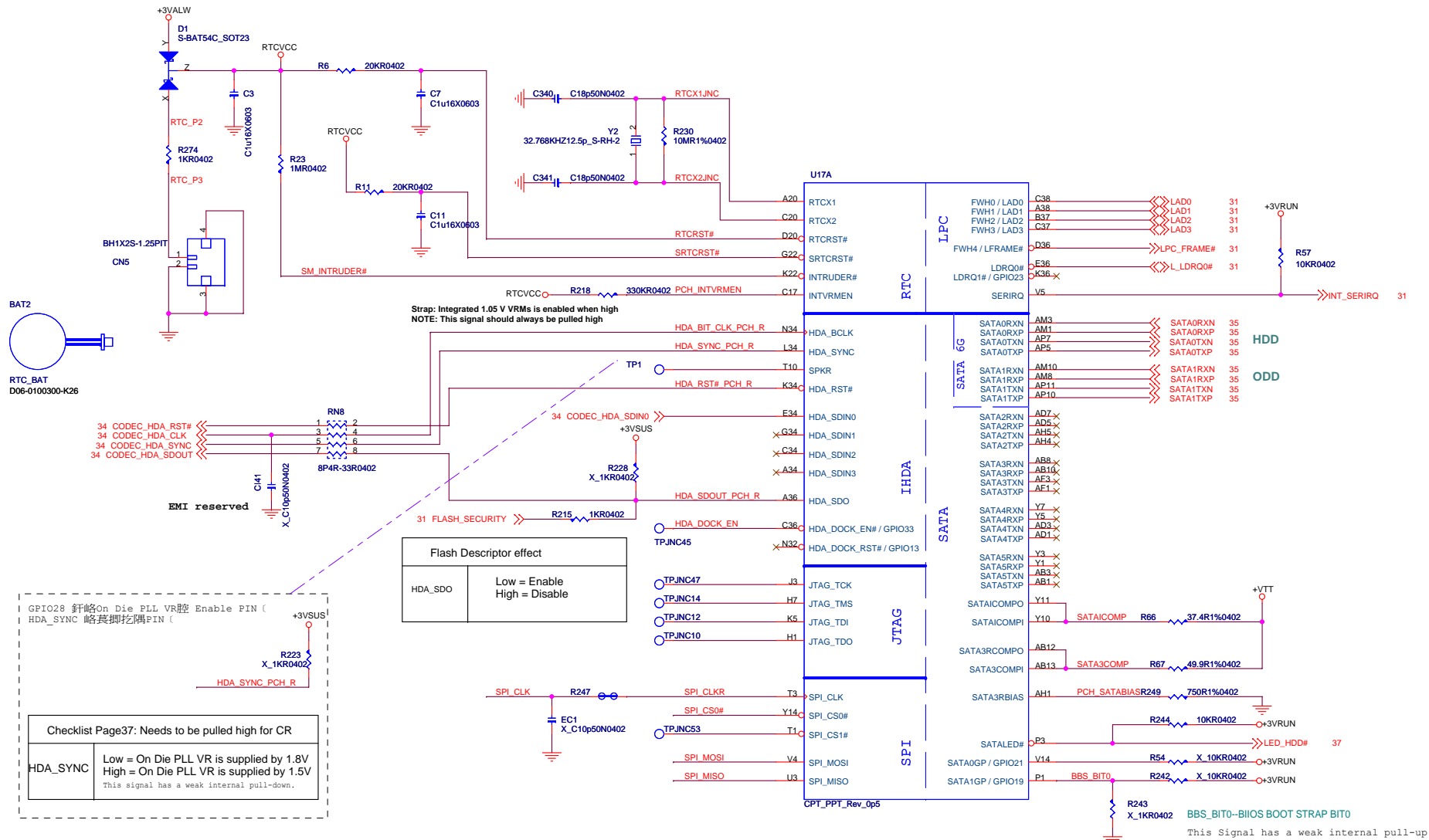
CALIBRATION PIN	DOR3 (ohm)
FB_CALx_PD_VDDQ	40.2
FB_CALx_PU_GND	42.2
FB_CALx_TERM_GND	51.1



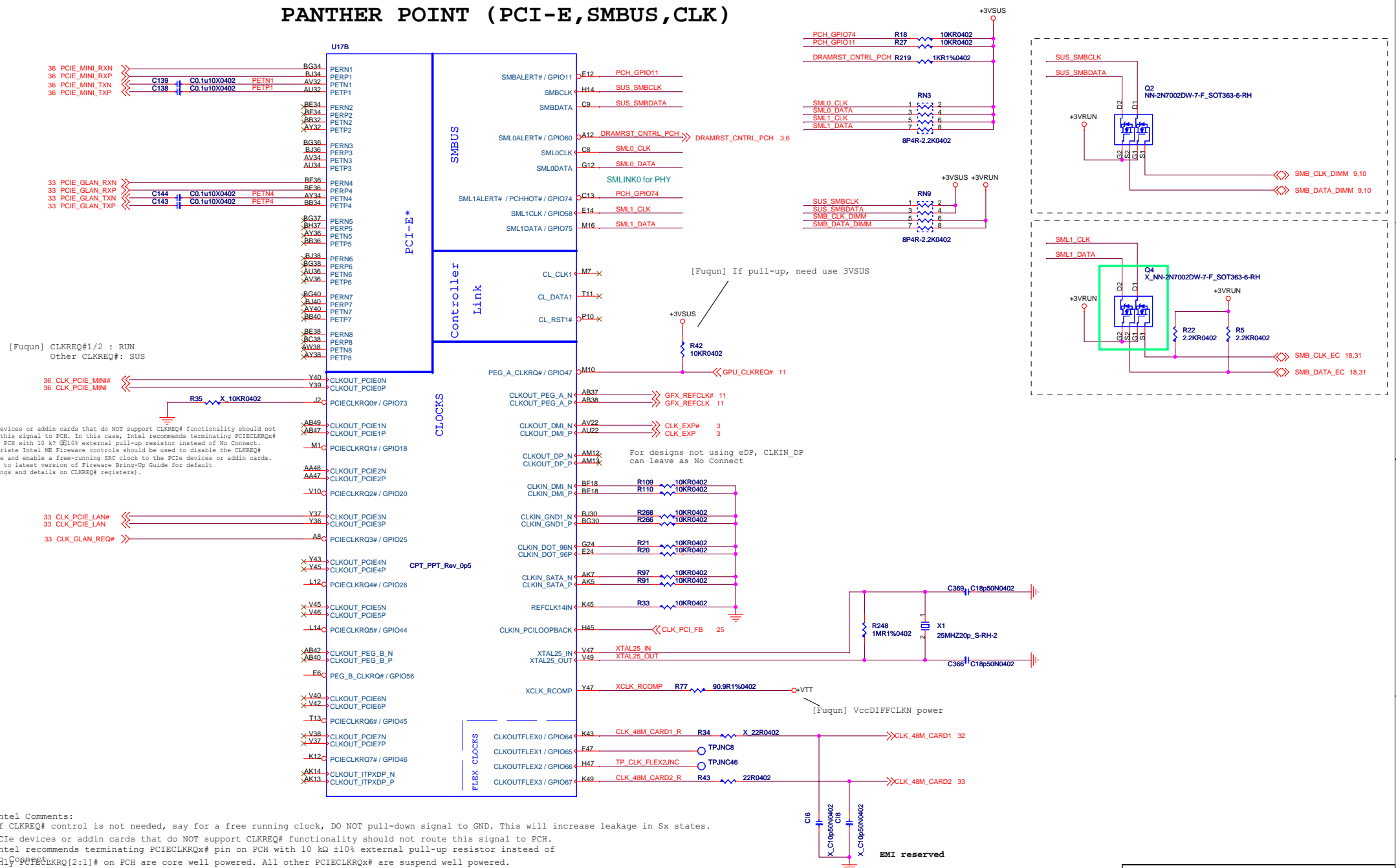


GPU Power Sequence

PANTHER POINT (HDA,JTAG,SATA)

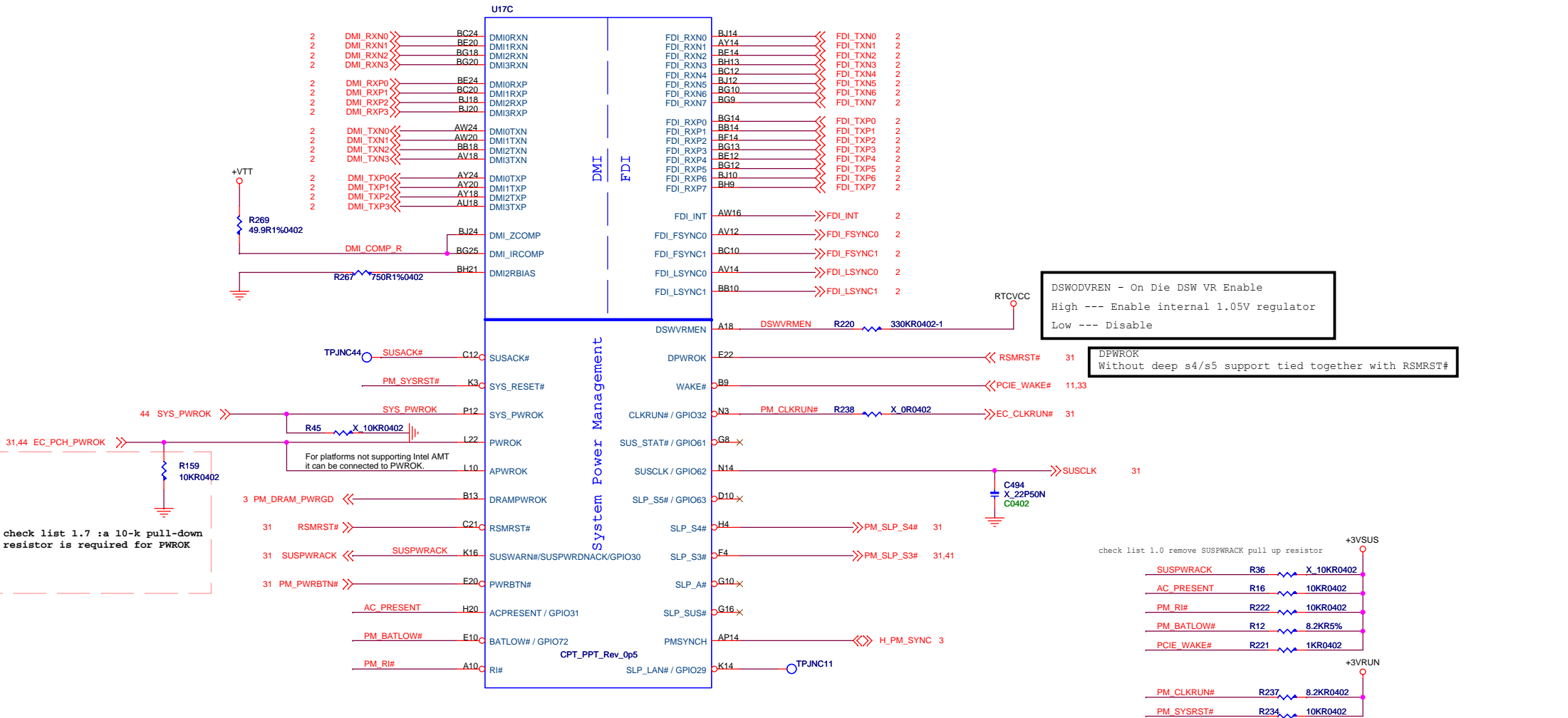


PANTHER POINT (PCI-E, SMBUS, CLK)



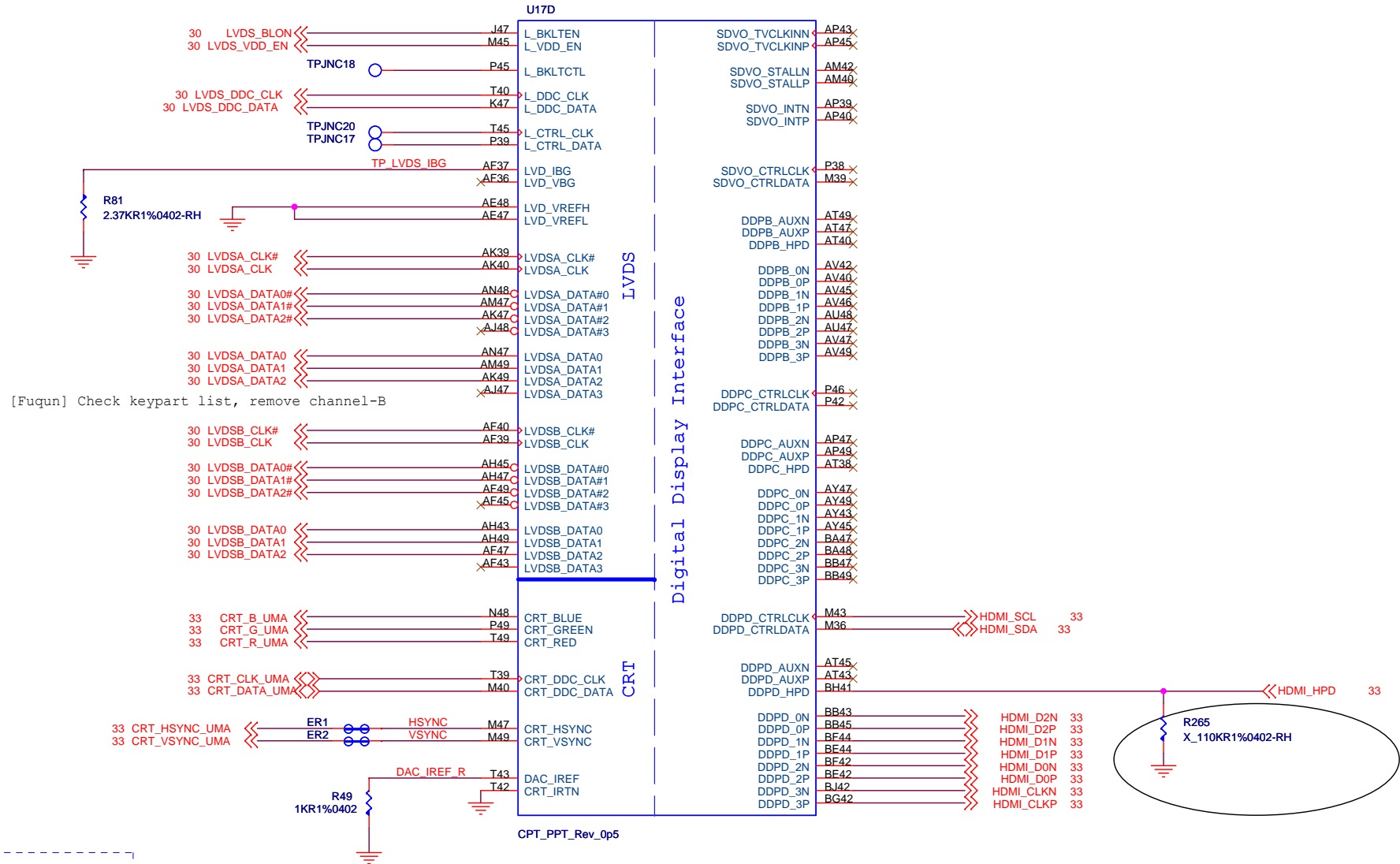
Title			
PCH-2 (PCI-E/SMBUS/CLK)			
Size	Document Number		Rev
Custom	MS-16GB		1.0
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PANTHER POINT (DMI, FDI, GPIO)

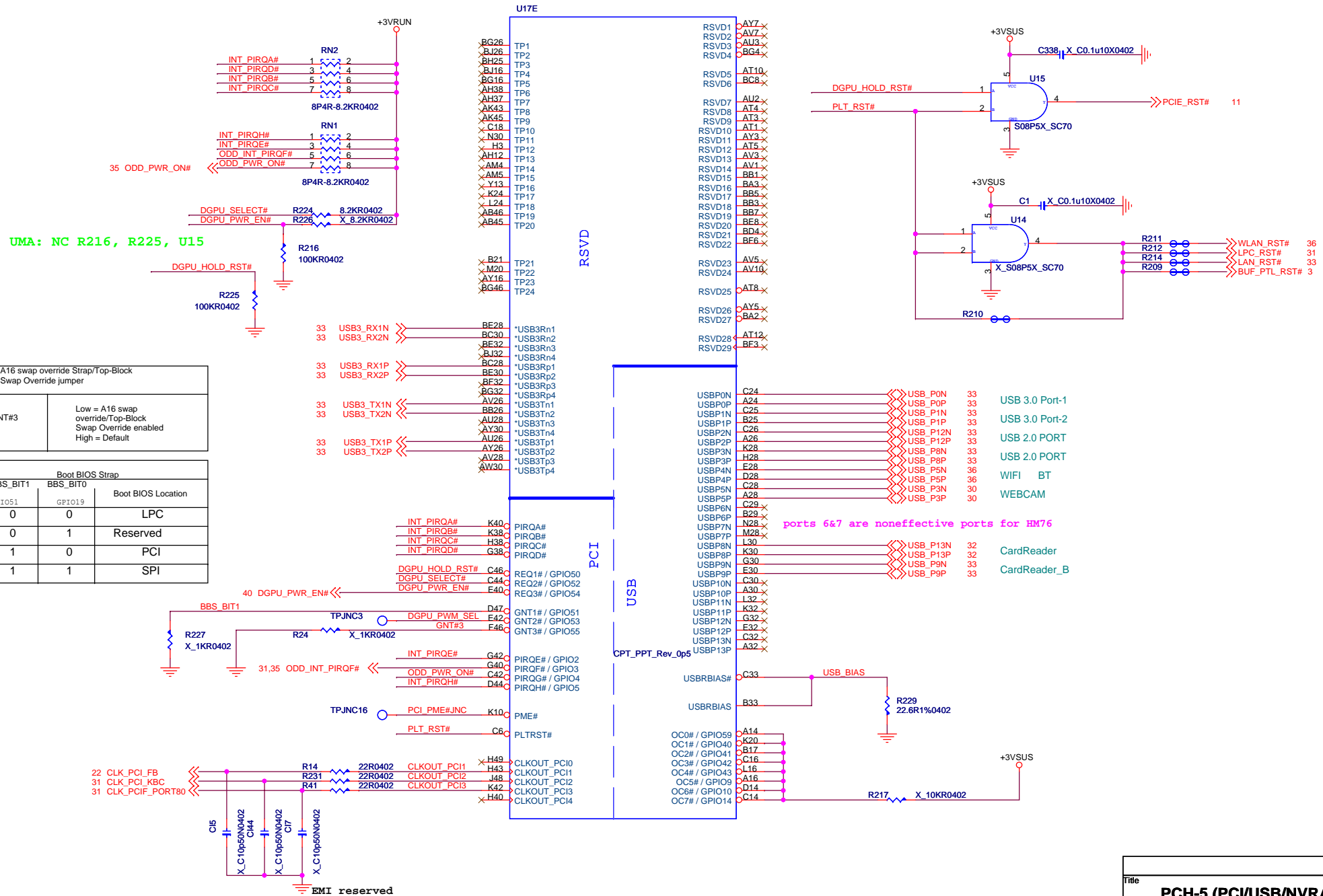


Title		
PCH-3 (DMI/FDI/GPIO)		
Size	Document Number	Rev
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PANTHER POINT (LVDS,DDI)

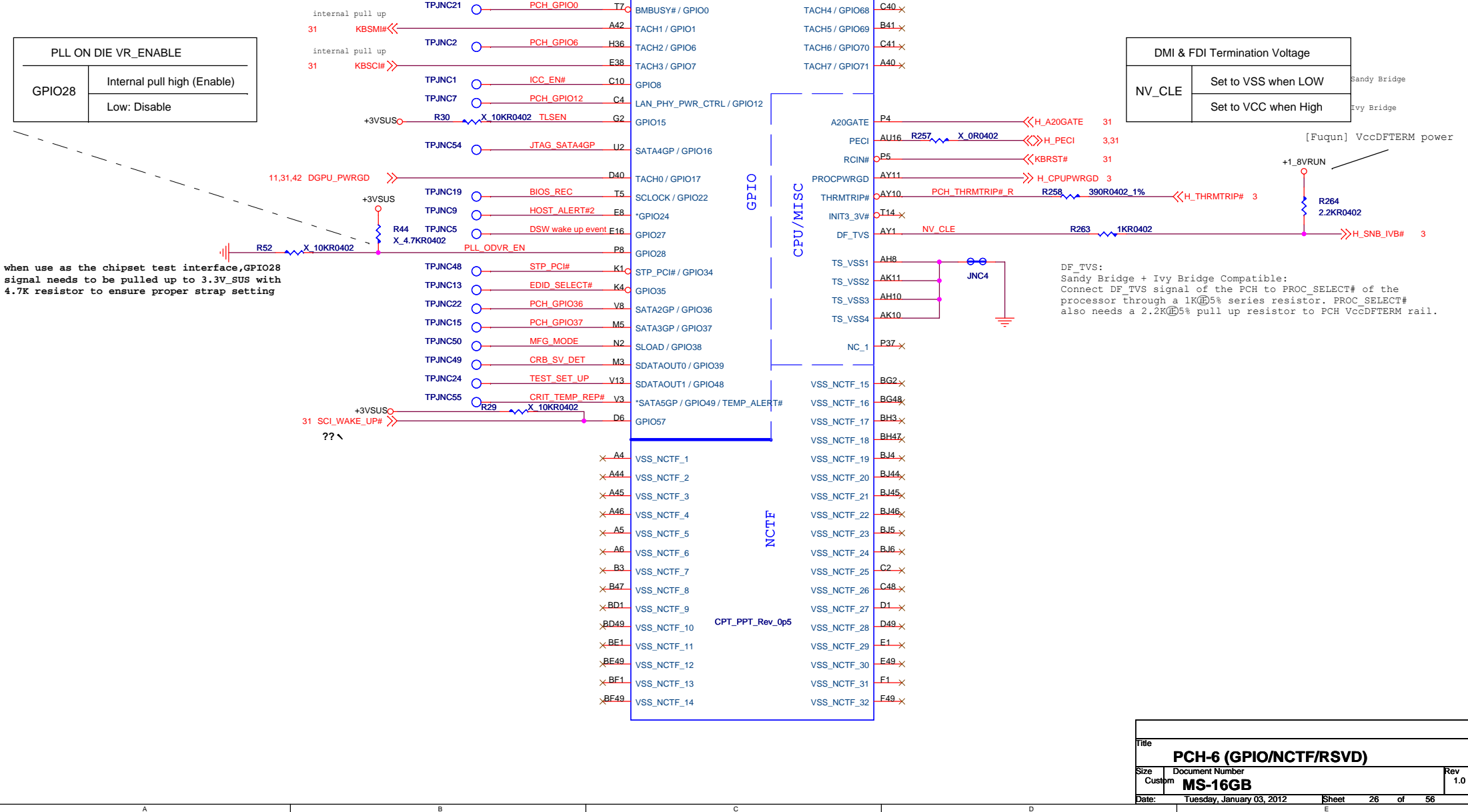


PANTHER POINT (PCI,USB,NVRAM)



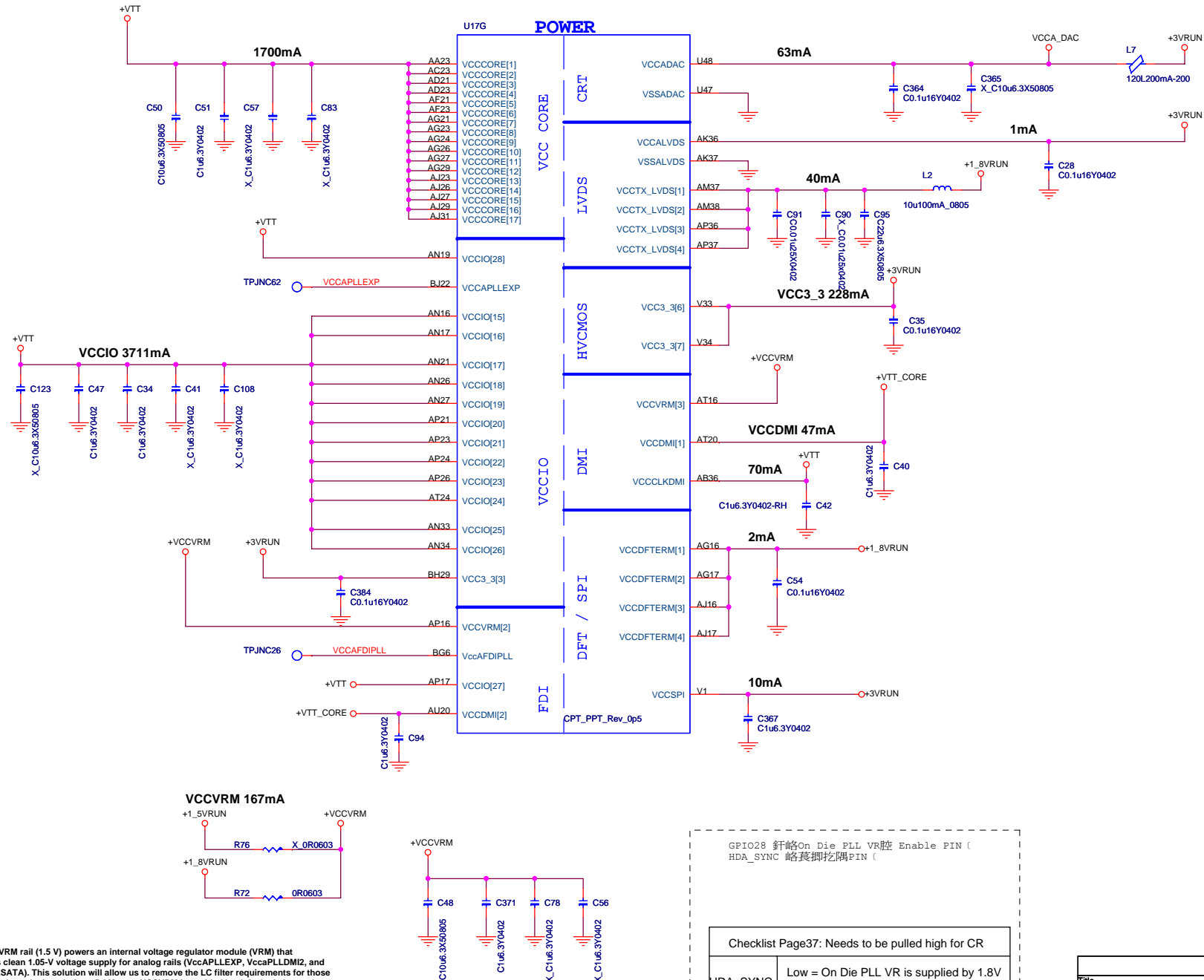
Title				
PCH-5 (PCI/USB/NVRAM)				
Size	Document Number			Rev
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PANTHER POINT (GPIO,VSS_NCTF,RSVD)



Title			PCH-6 (GPIO/NCTF/RSVD)	
Size	Custom	Document Number	MS-16GB	
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		Rev	1.0	

PANTHER POINT (POWER)

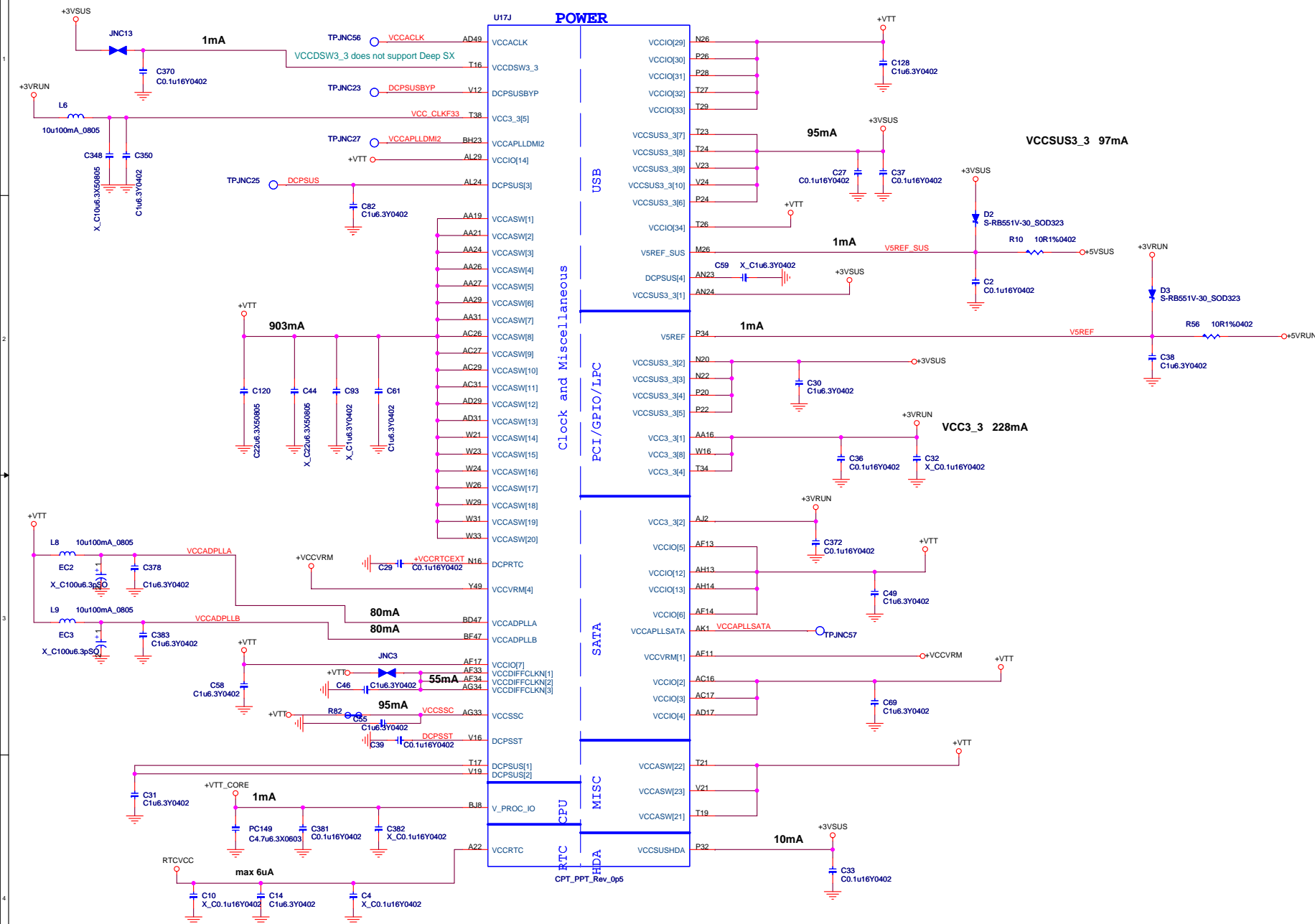


GPI028 針路On Die PLL VR腔 Enable PIN (HDA_SYNC 略長抑挖隔PIN (

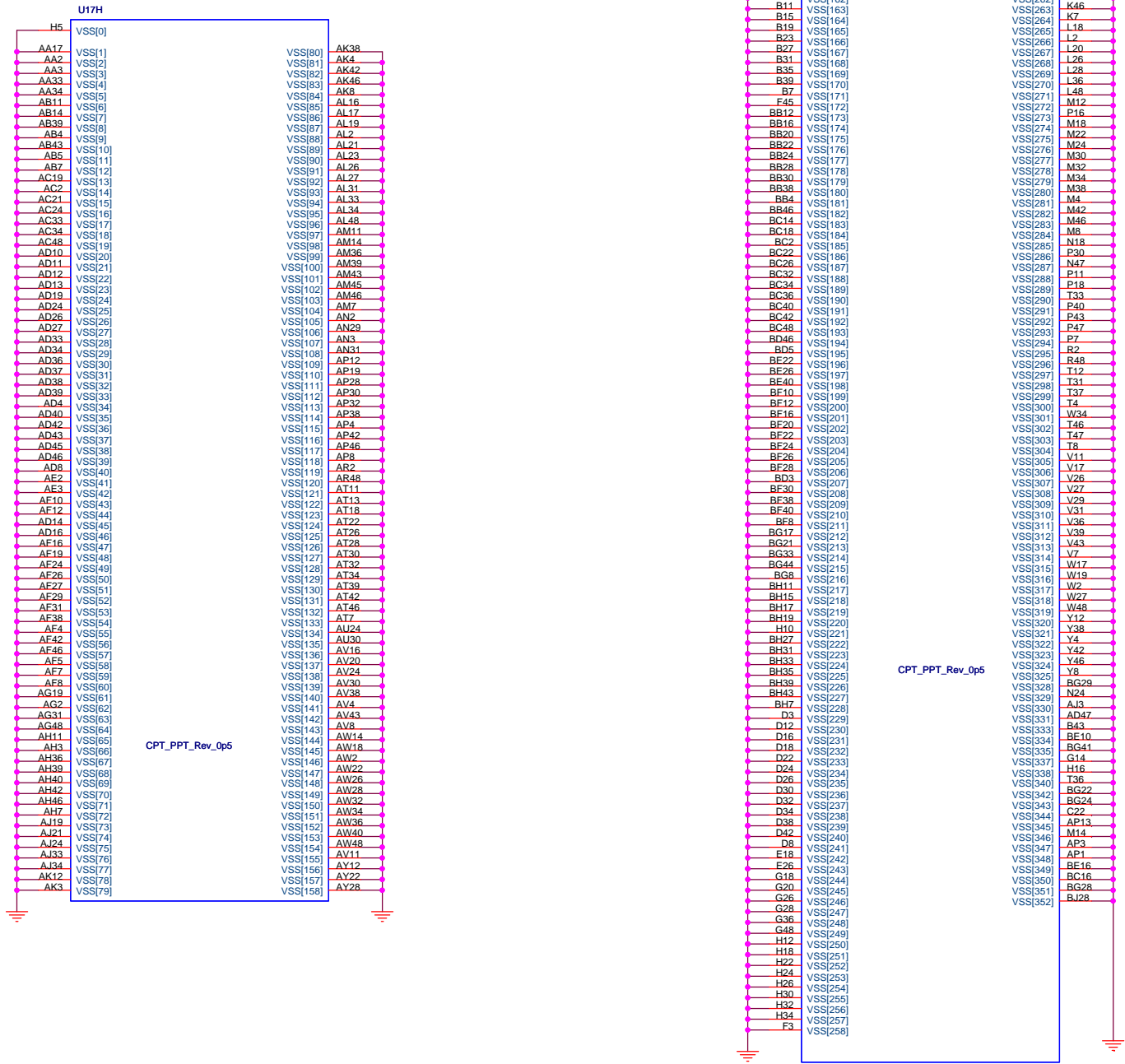
Checklist Page37: Needs to be pulled high for CR	
HDA_SYNC	Low = On Die PLL VR is supplied by 1.8V High = On Die PLL VR is supplied by 1.5V This signal has a weak internal pull-down.

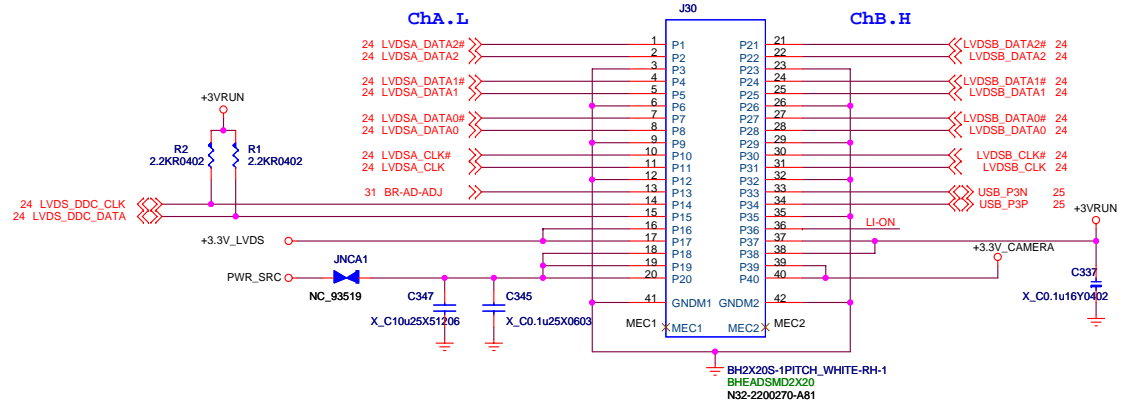
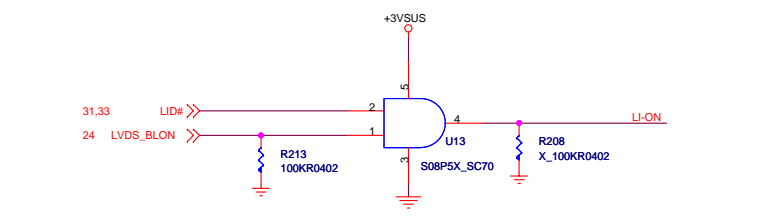
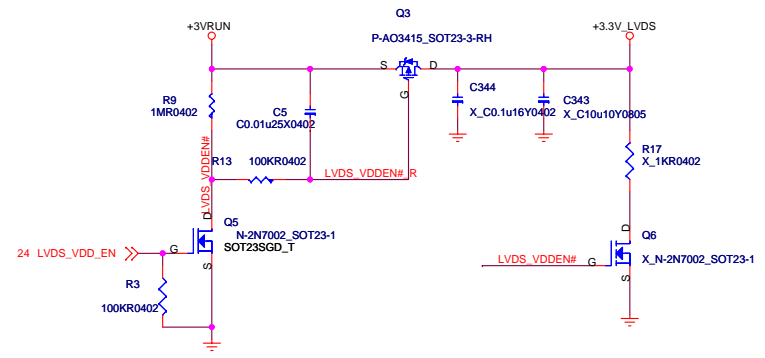
The VCCVRM rail (1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VccAPLLEXP, VccAPLLDMI2, and VccAPLLSATA). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO28,

PANTHER POINT (POWER)

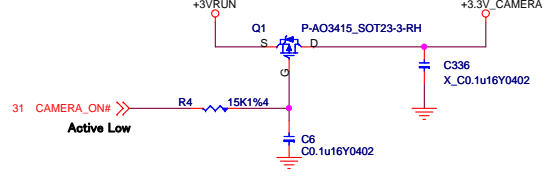



PANTHER Point (GND)

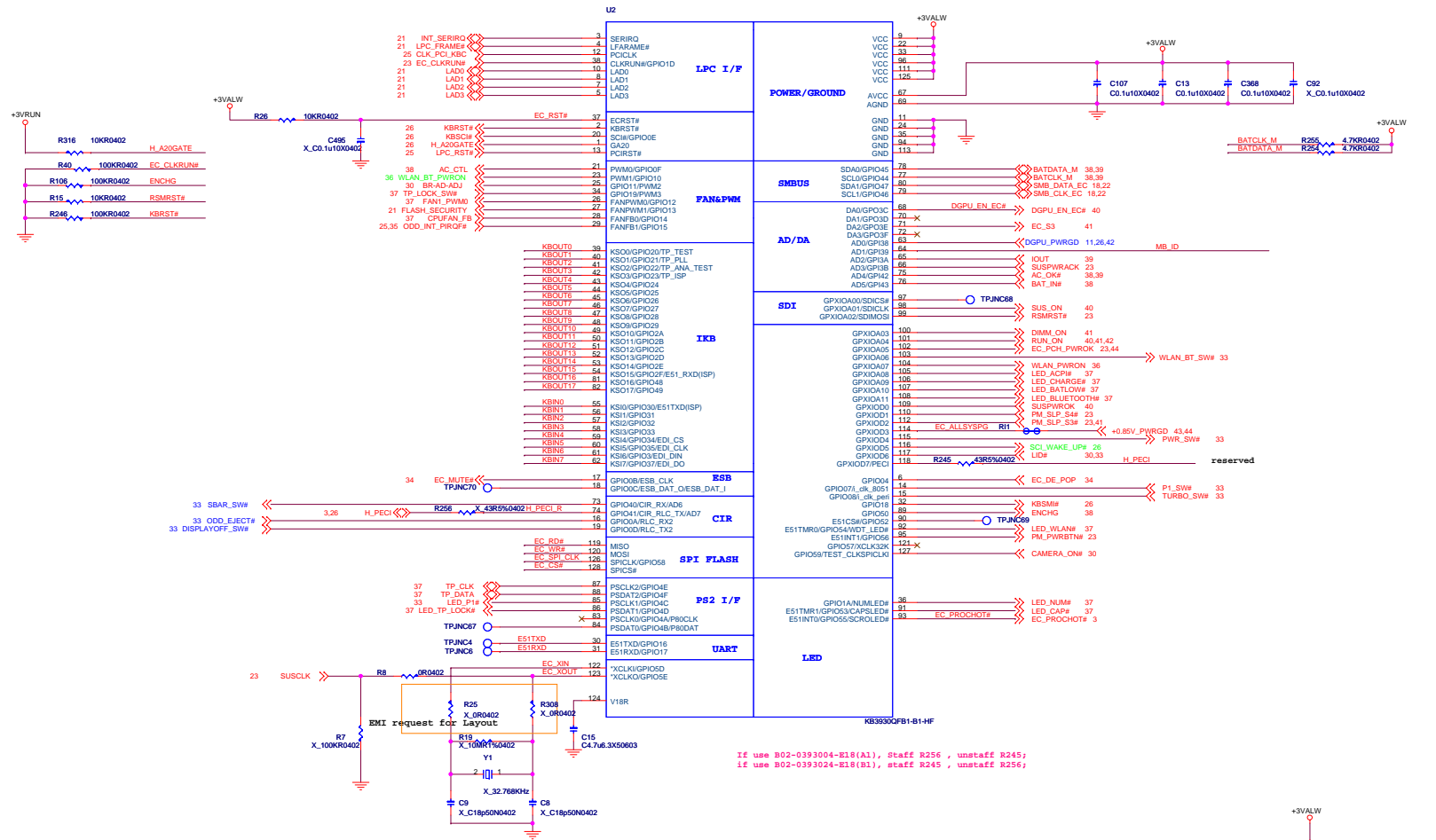




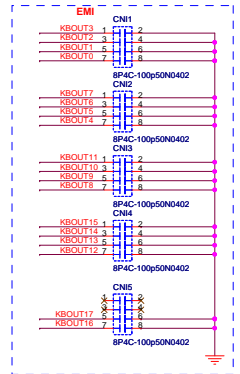
CAMERA



 <small>Lead the Way to Your Computer</small>		MICRO-STAR INT'L CO.,LTD.	
Title			
LVDS, Camera			
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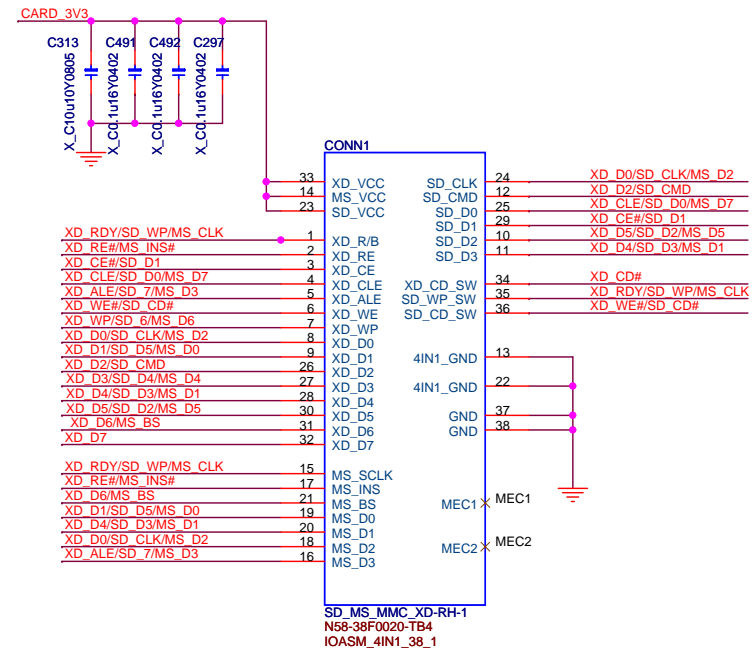
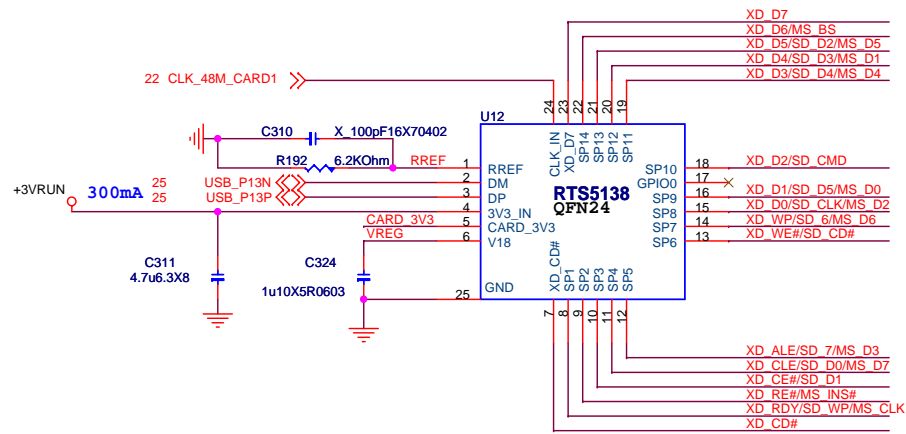


If use B02-0393004-E18(A1), staff R256 , unstaff R245;
 If use B02-0393024-E18(B1), staff R245 , unstaff R256;

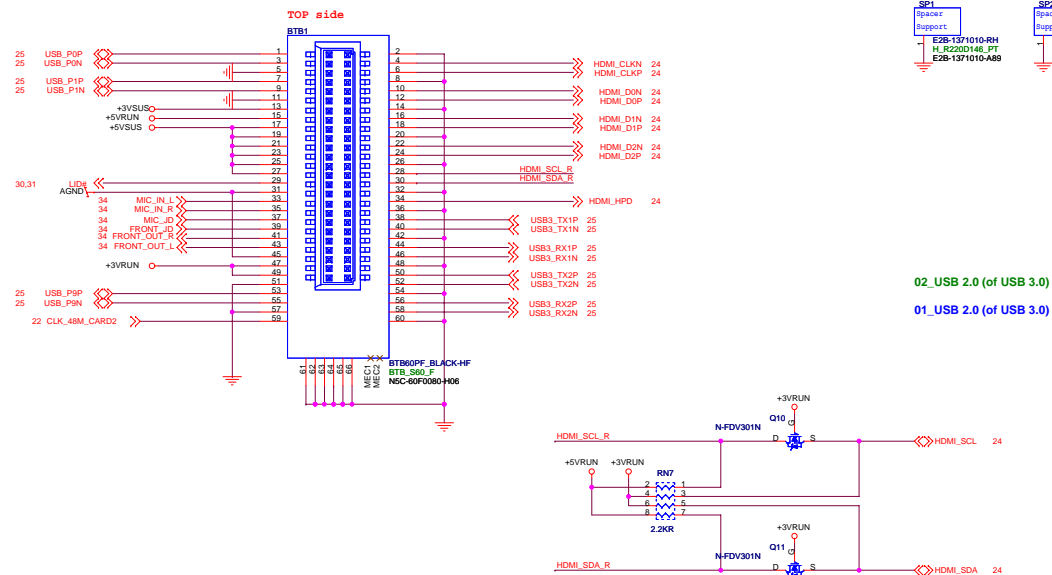


Card Reader controller RTS5138

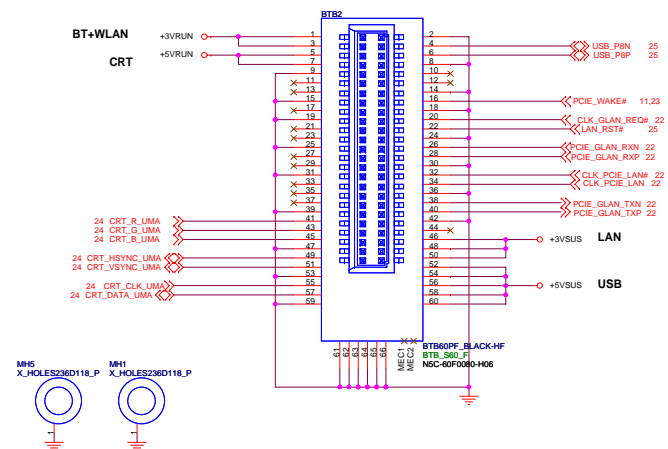
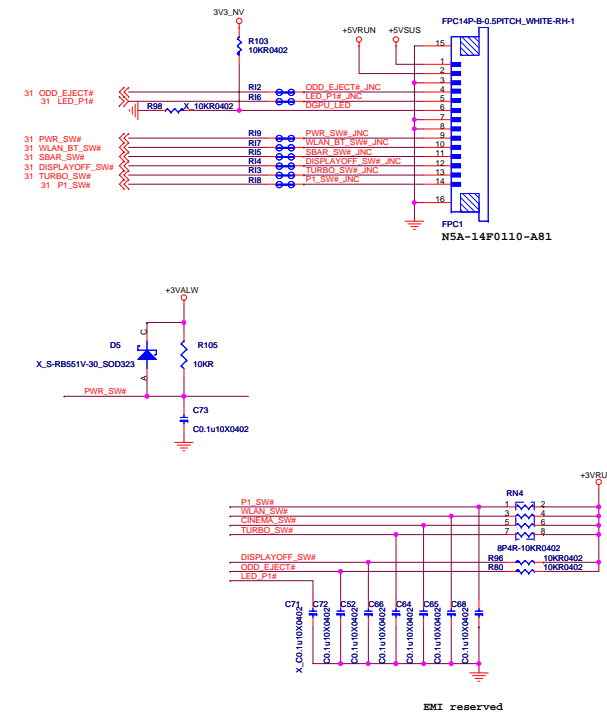
CFG for 16GB

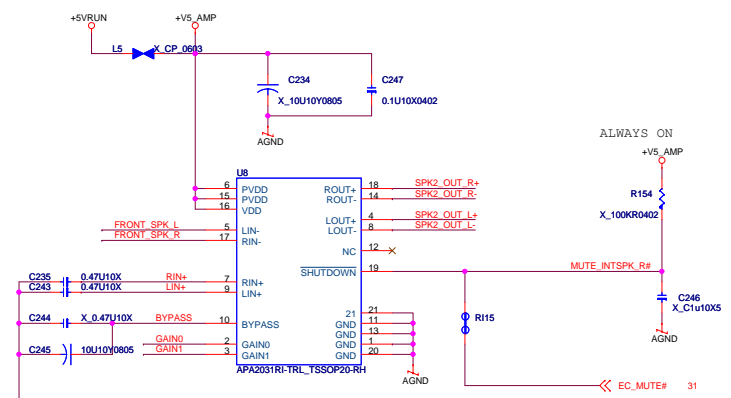
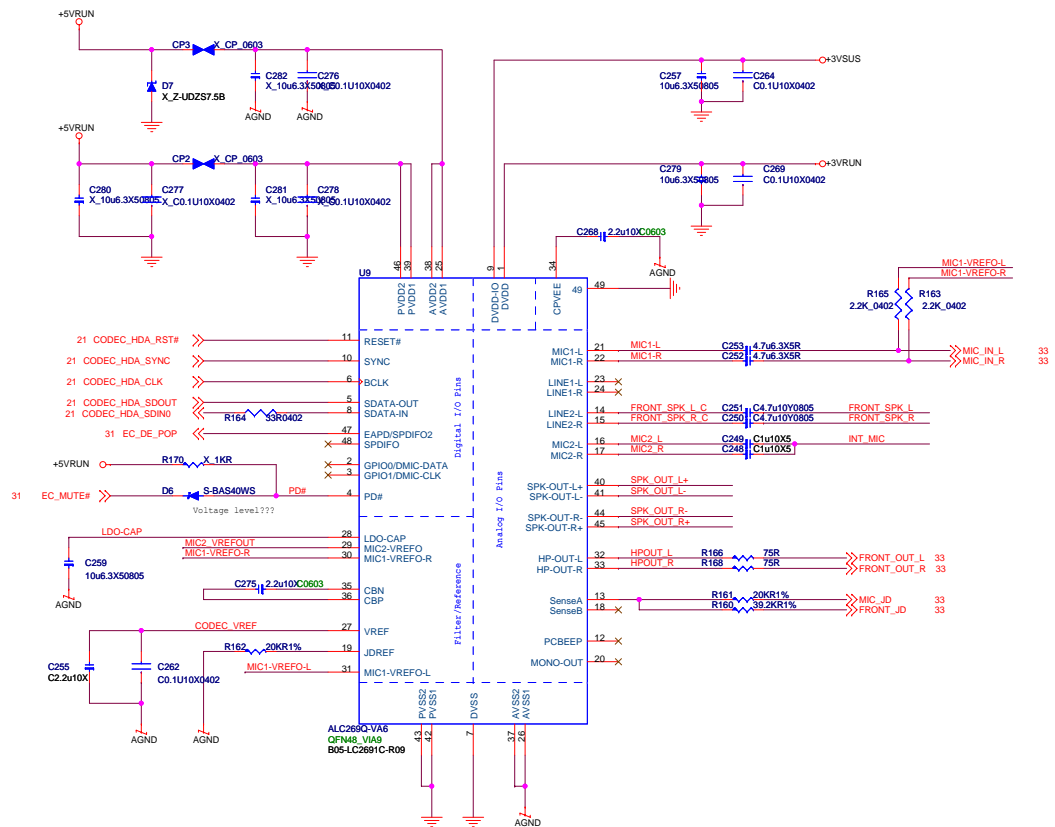


[A] board: USB,LAN,CRT,BT+WLAN

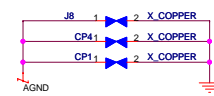
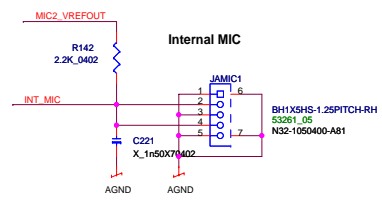
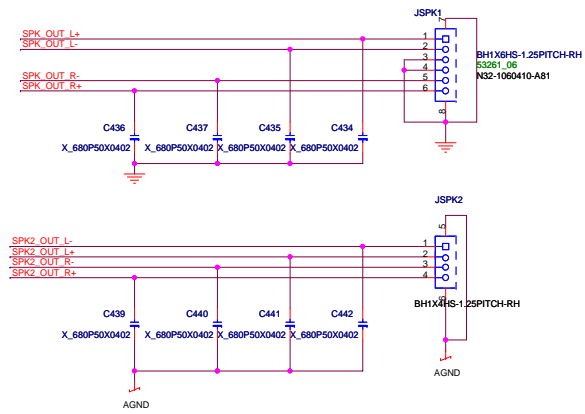
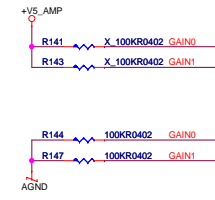


For 175X [E] board

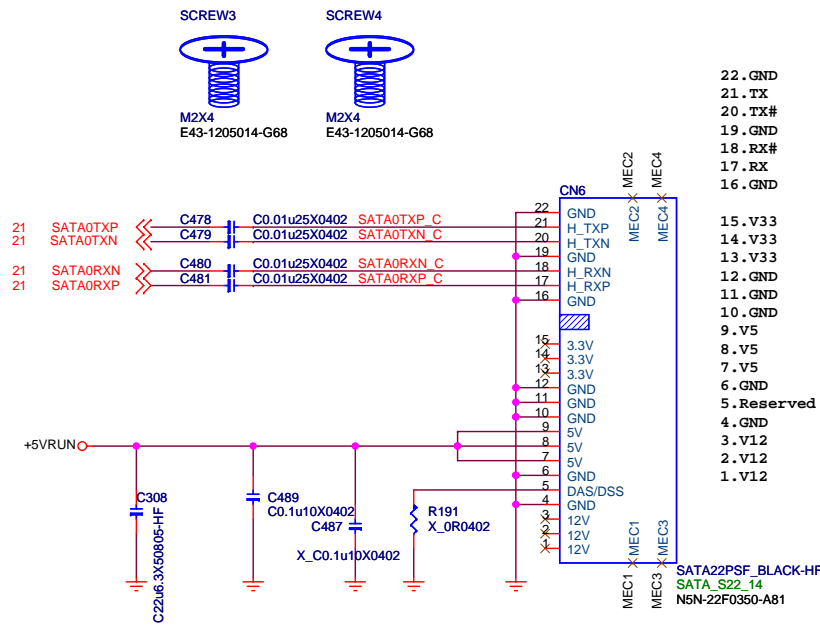




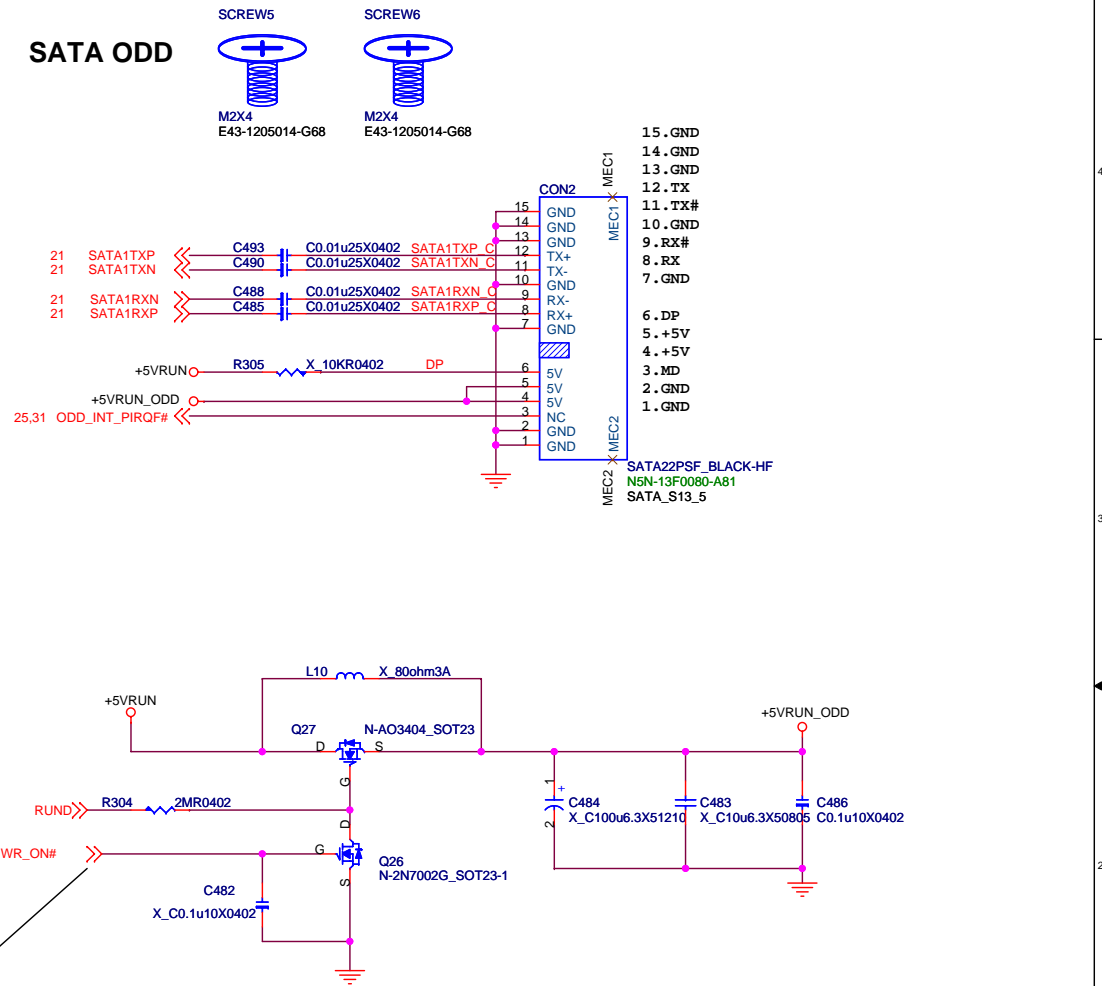
For APA2031			For FAN7031			
Av	GAIN0	GAIN1	Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	6dB	0	0	0
10dB	0	1	10dB	0	1	0
15.6dB	1	0	15.6dB	1	0	0
21.6dB	1	1	21.6dB	1	1	0
4.3dB	X	X	4.3dB	X	X	1



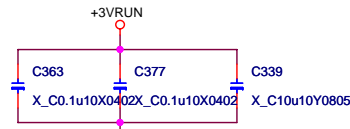
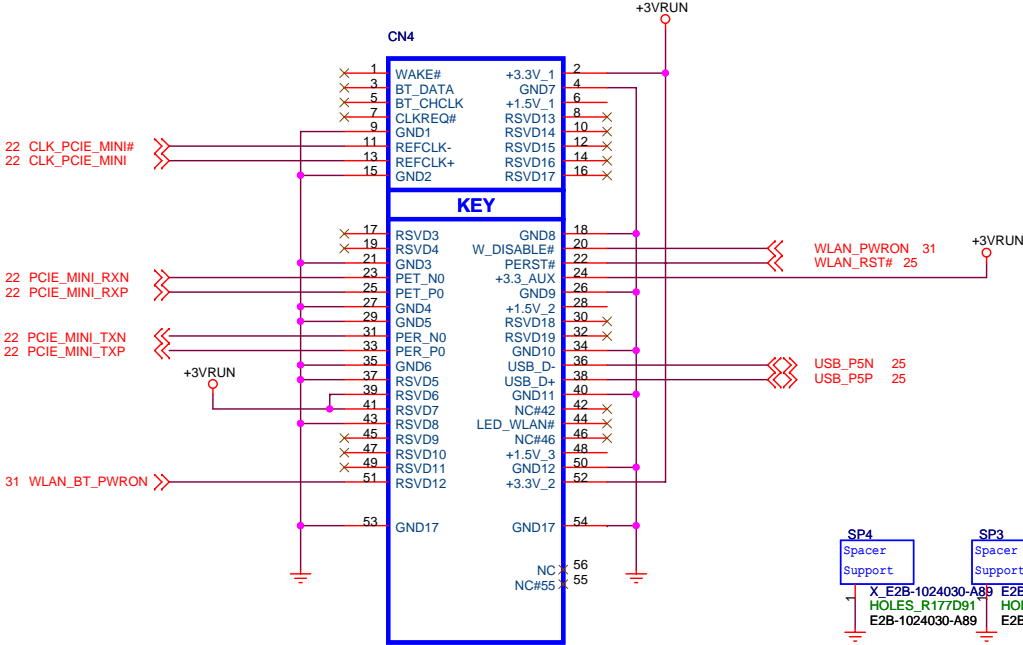
SATA HDD



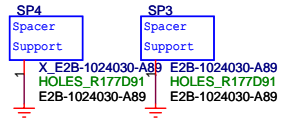
SATA ODD



WLAN



delete 1.5vrun because no wireless card in product AVL
use this voltage

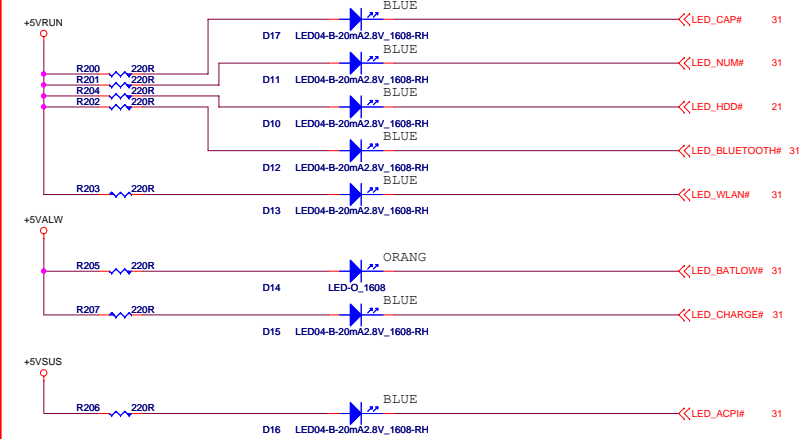


PIN51 for intel N130 BT control &AW-NB087H BT control;
PIN5 for AW-NB041H BT control;
AW-NB087H BT do not use USB interface,it only share PCIE interface.

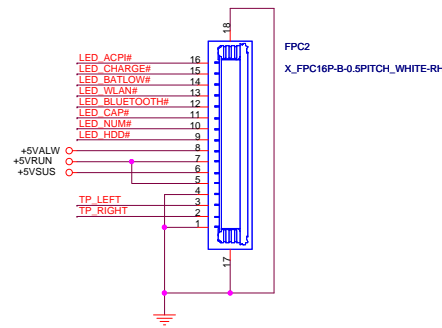
below WLAN cards are have been
checked which can be used :
Intel N130/N135;
AW-NB100H/NE785H/NE139H;

LED

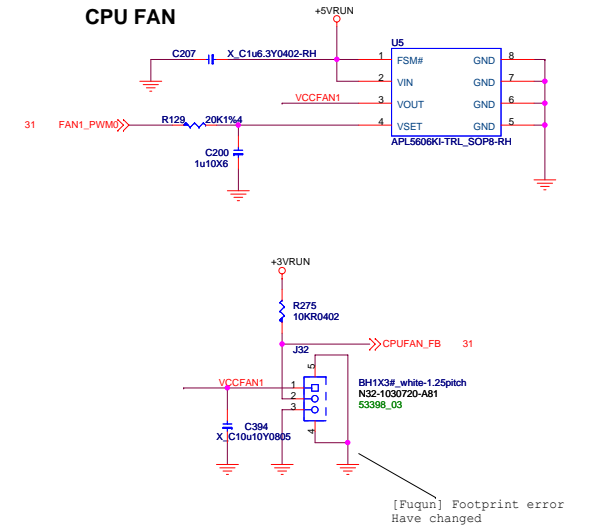
For 16GX



For 175X [D] board

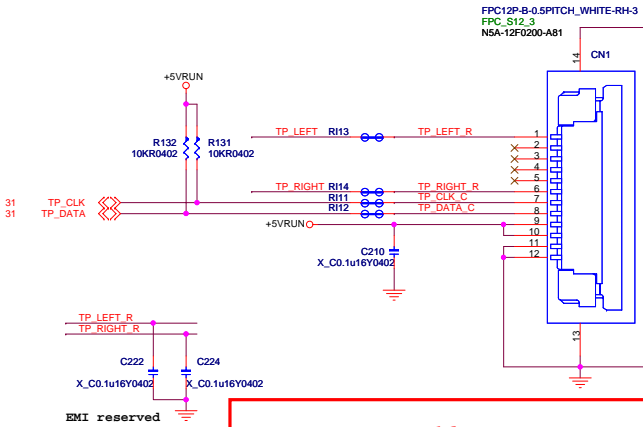


CPU FAN

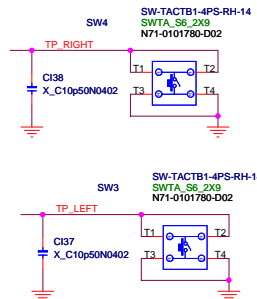
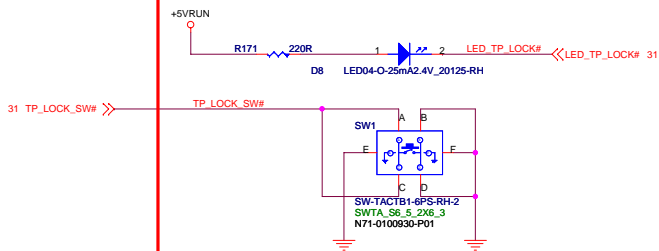


[Fugun] Footprint error
Have changed

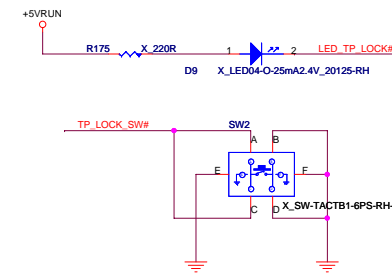
Touch Pad

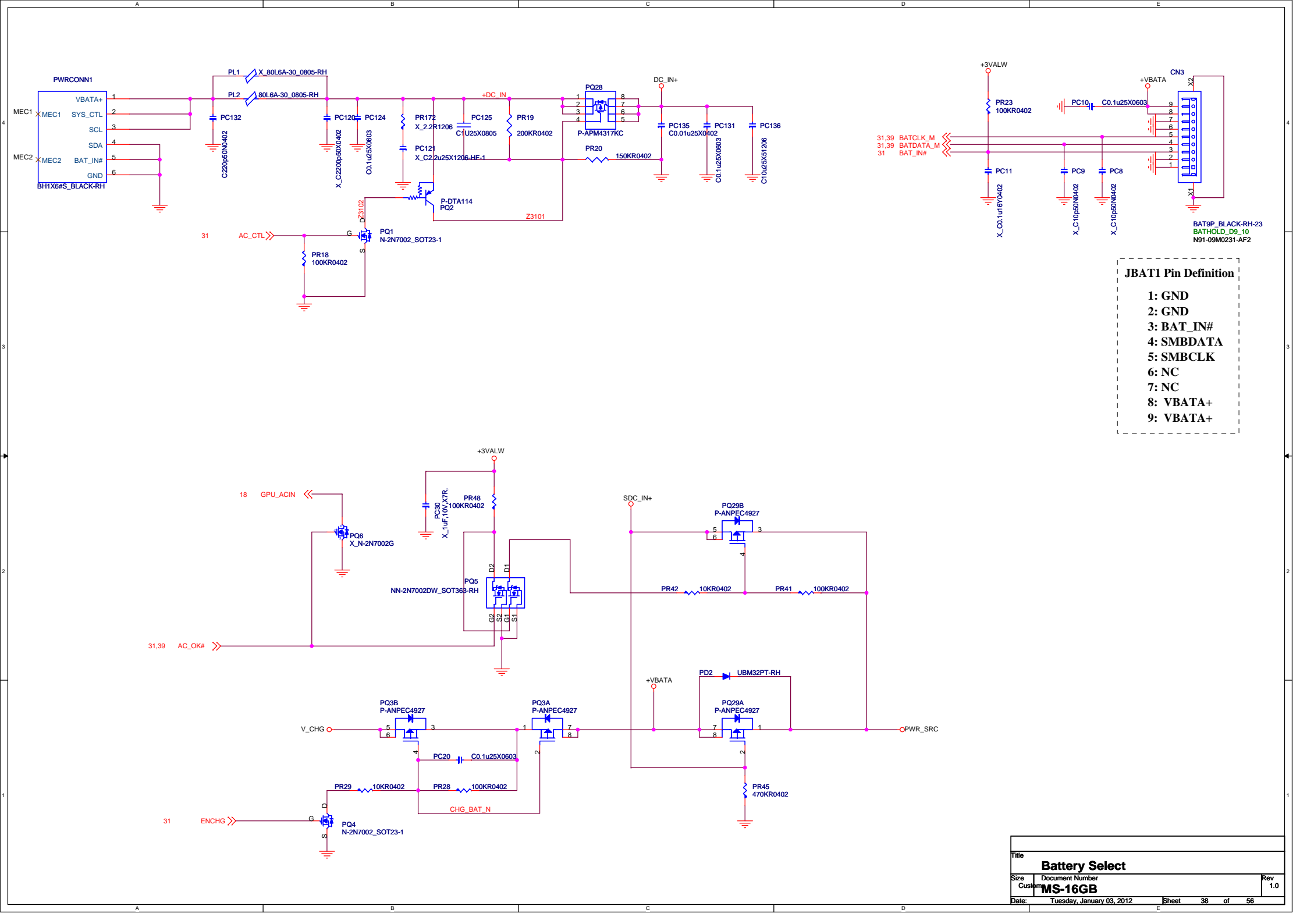


For 16GB



For 175X

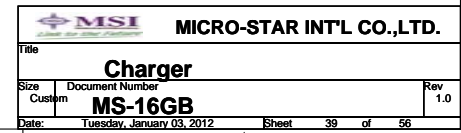


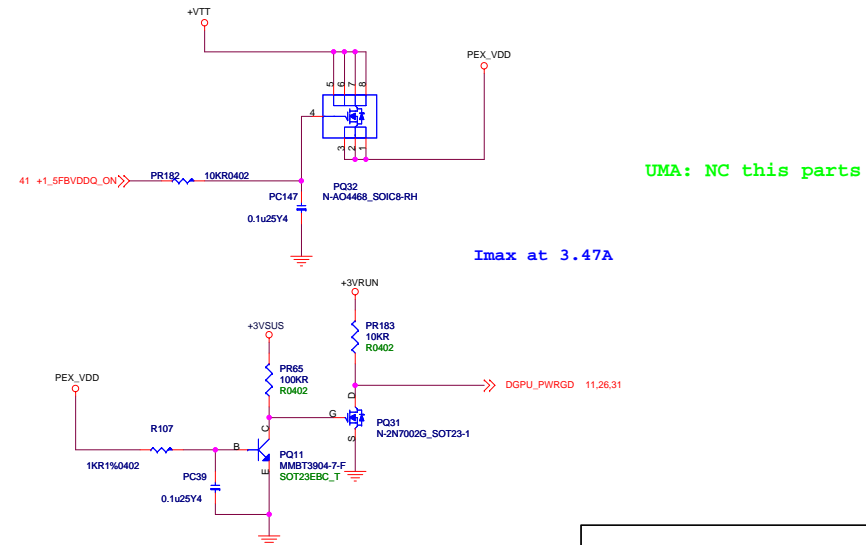
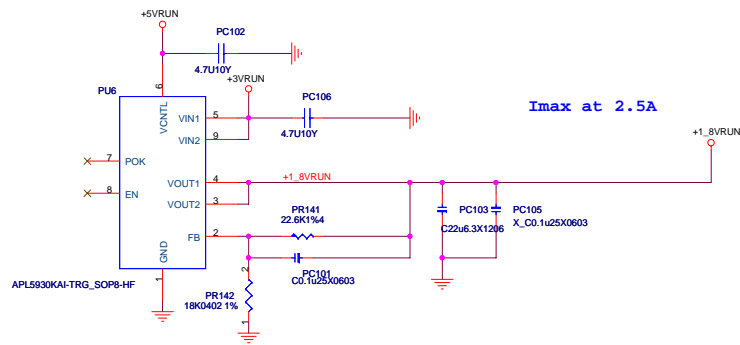
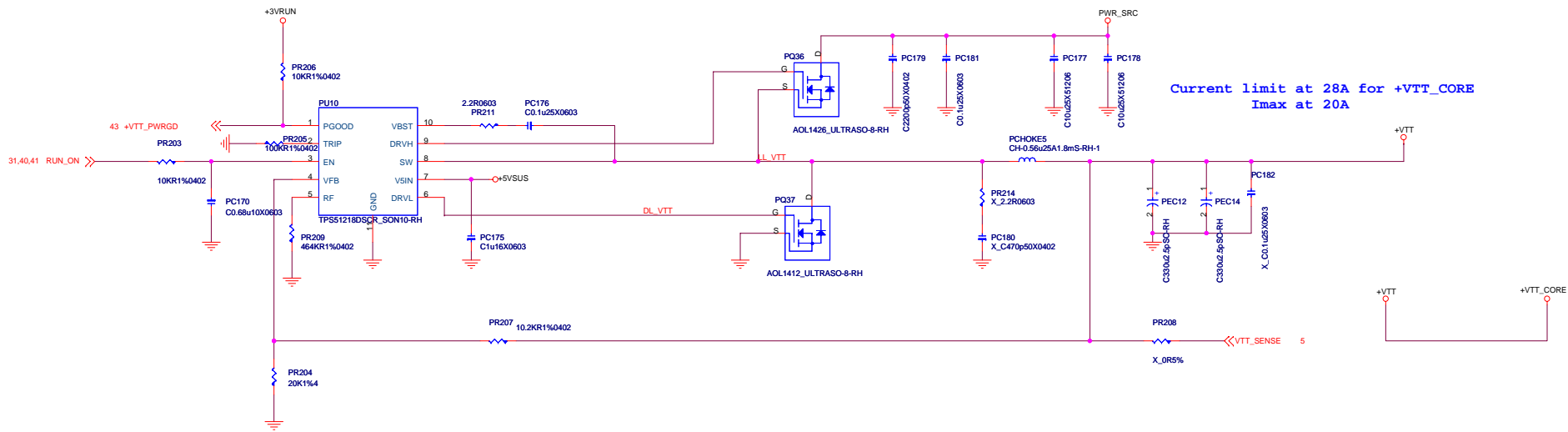


JBAT1 Pin Definition

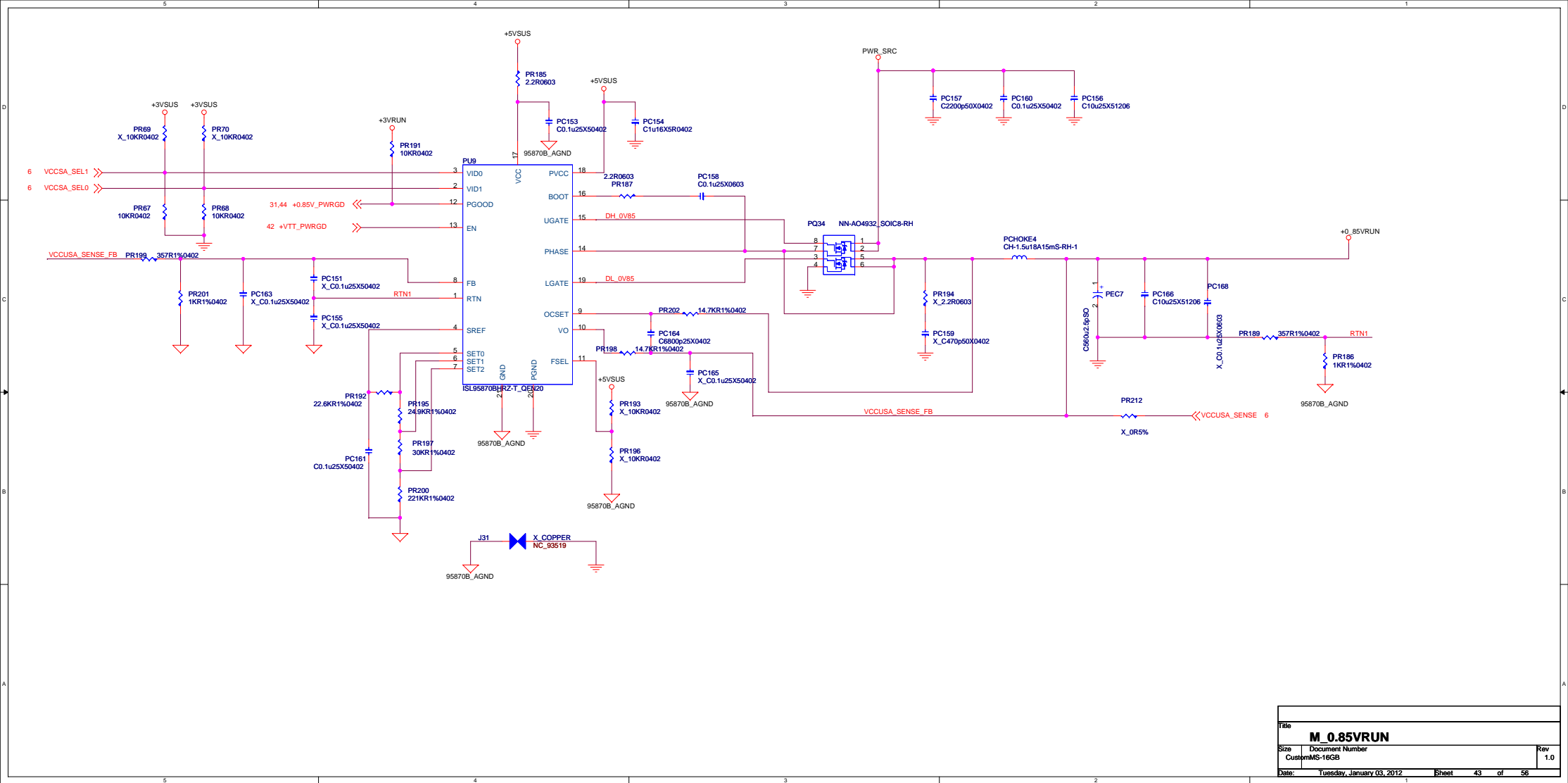
- 1: GND
- 2: GND
- 3: BAT_IN#
- 4: SMBDATA
- 5: SMBCLK
- 6: NC
- 7: NC
- 8: VBATA+
- 9: VBATA+

Adapter input voltage set 19 Voltage

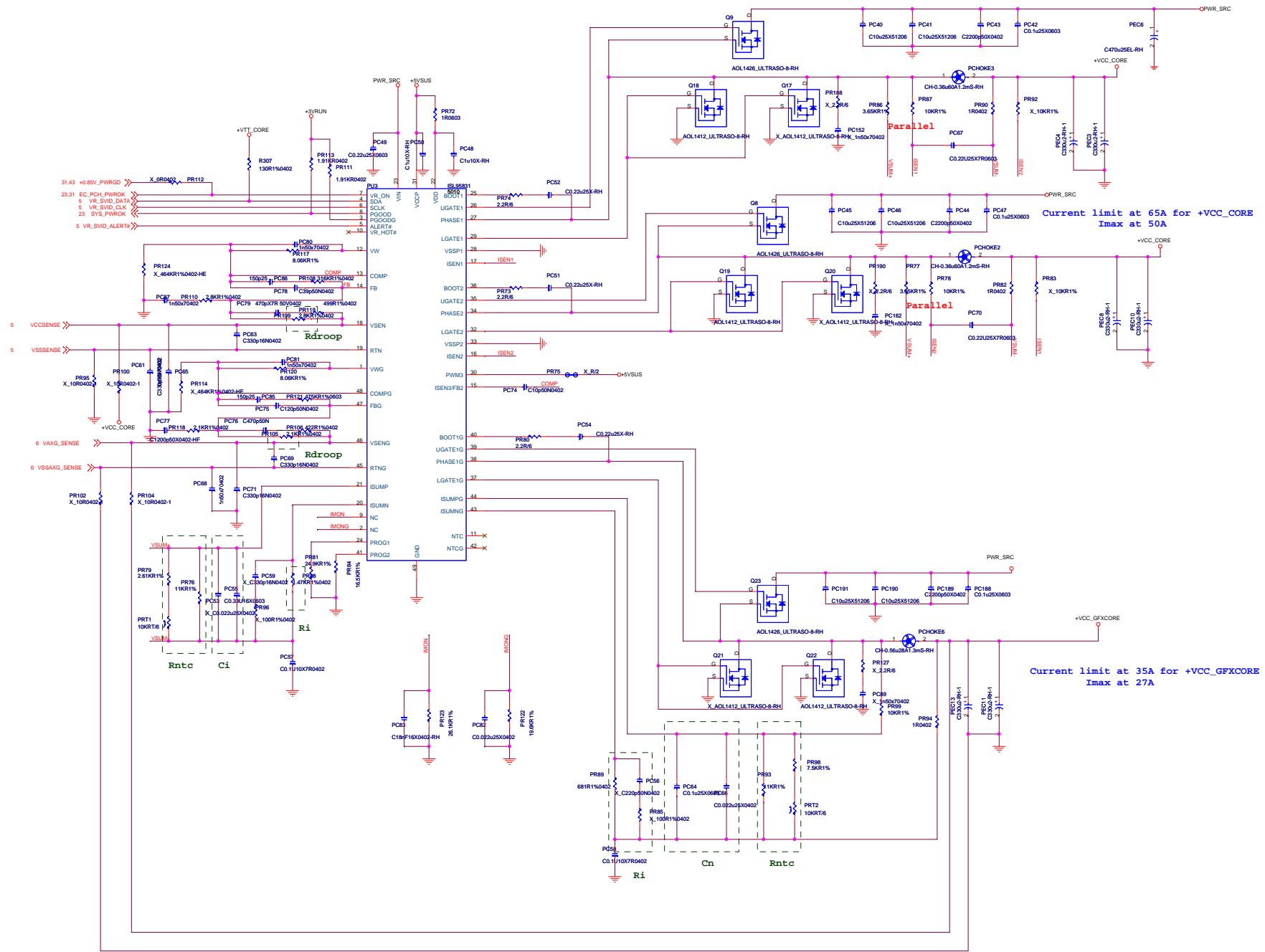


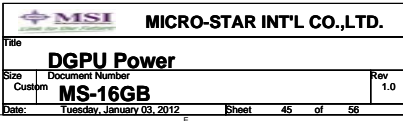


Title		
VTT_1.8V_RUN		
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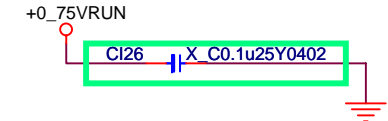
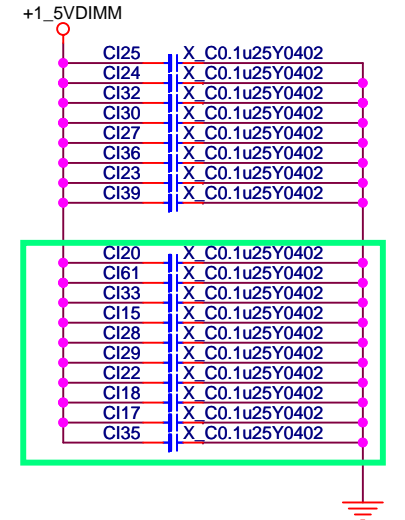
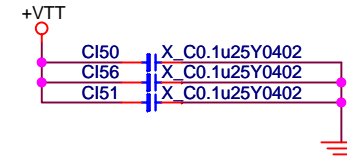
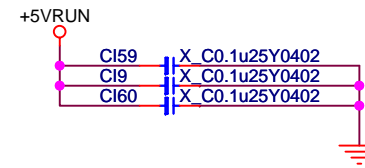
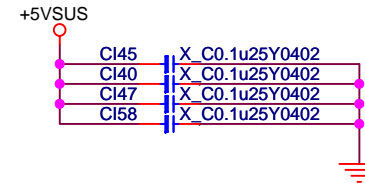
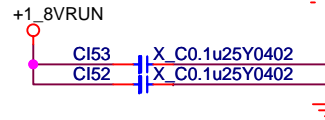
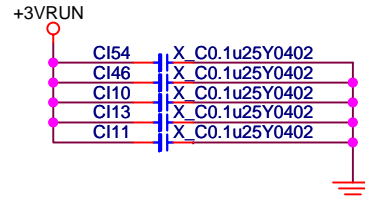
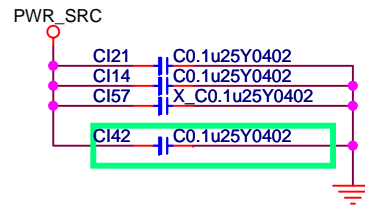
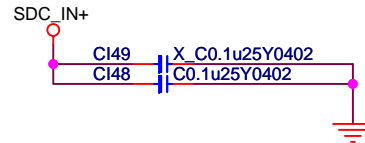
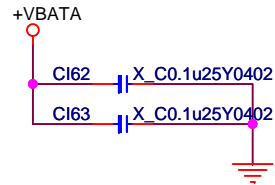
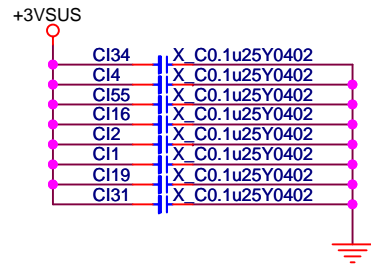
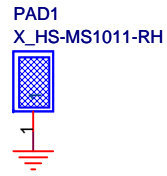
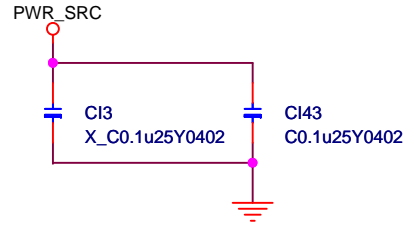
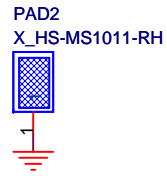



Title		
M_0.85VRUN		
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Custom	MMS-16GB	1.0
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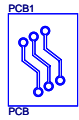
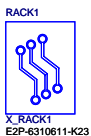
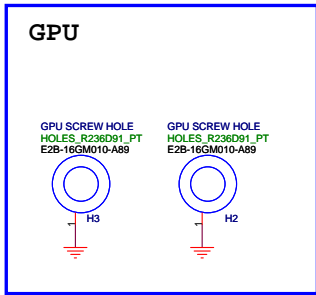
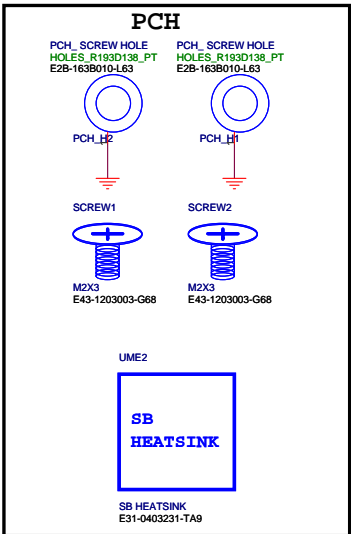
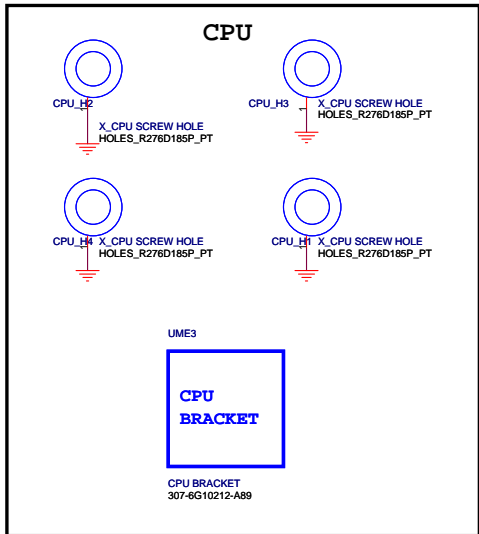
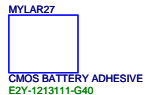
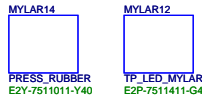
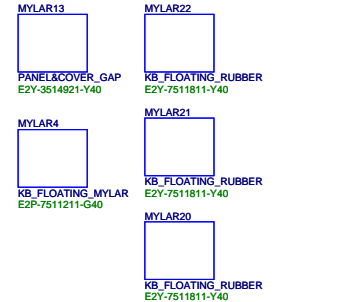
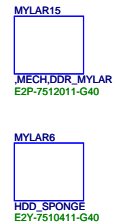
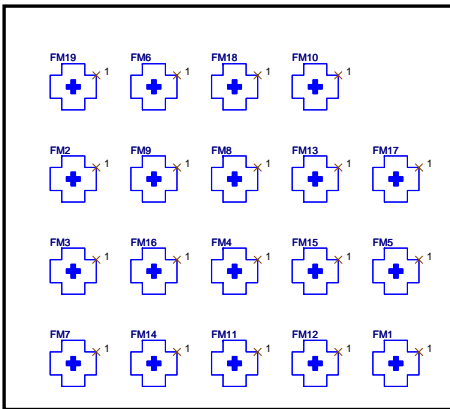
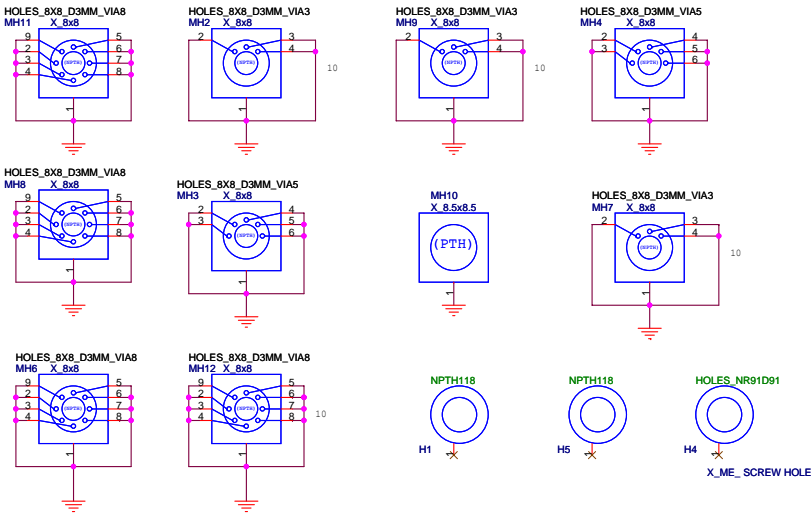




BOT SPRING



 MICRO-STAR INT'L CO.,LTD.	
Title	
EMI	
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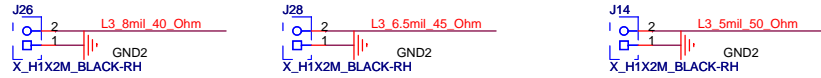


Single-end

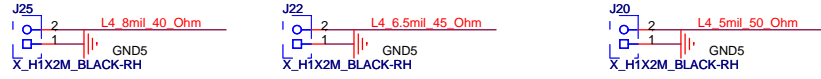
TOP



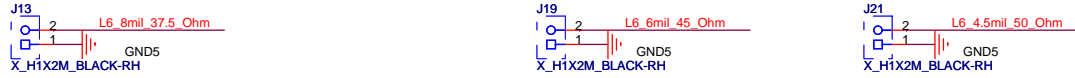
IN3



IN4

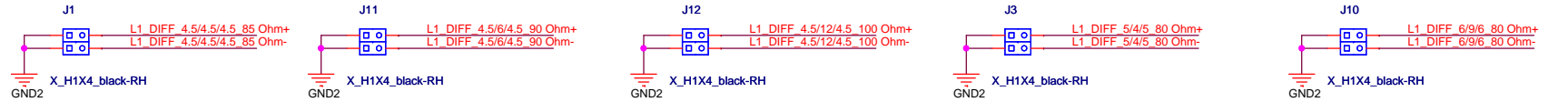


BOTTOM



Differential signal

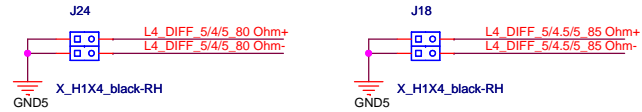
TOP



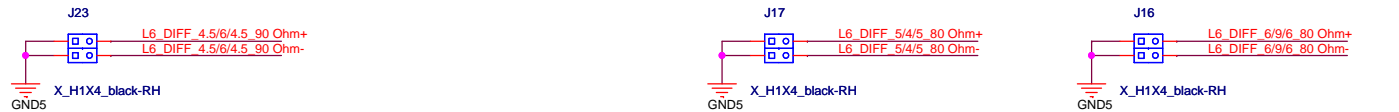
IN3



IN4

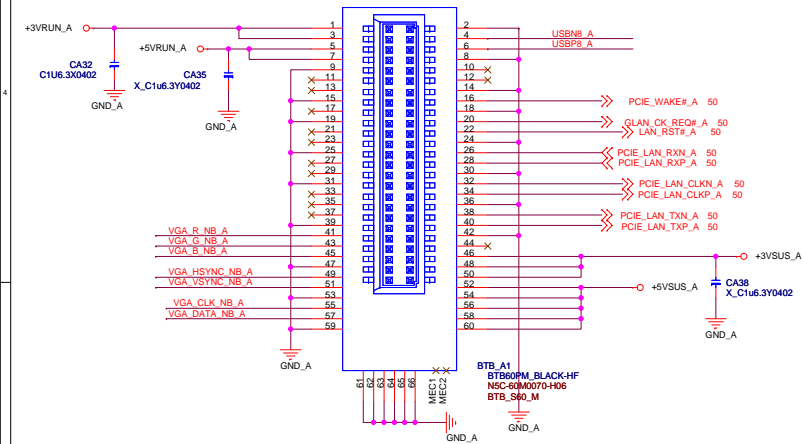


BOTTOM

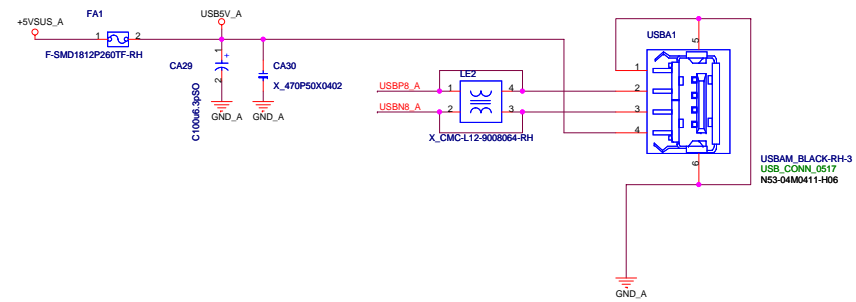


Title			
Impedance			
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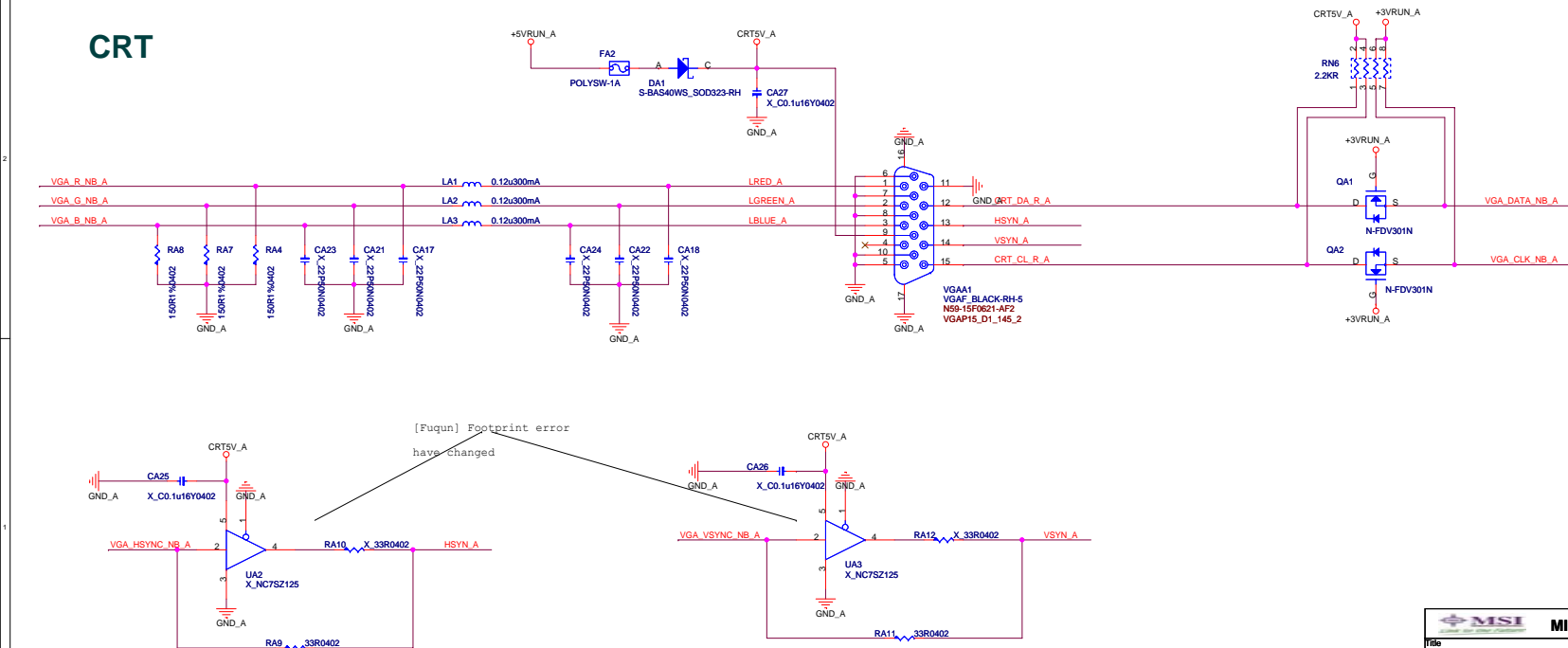
60PIN BTB I/O Connector(VGA, LAN, USB)

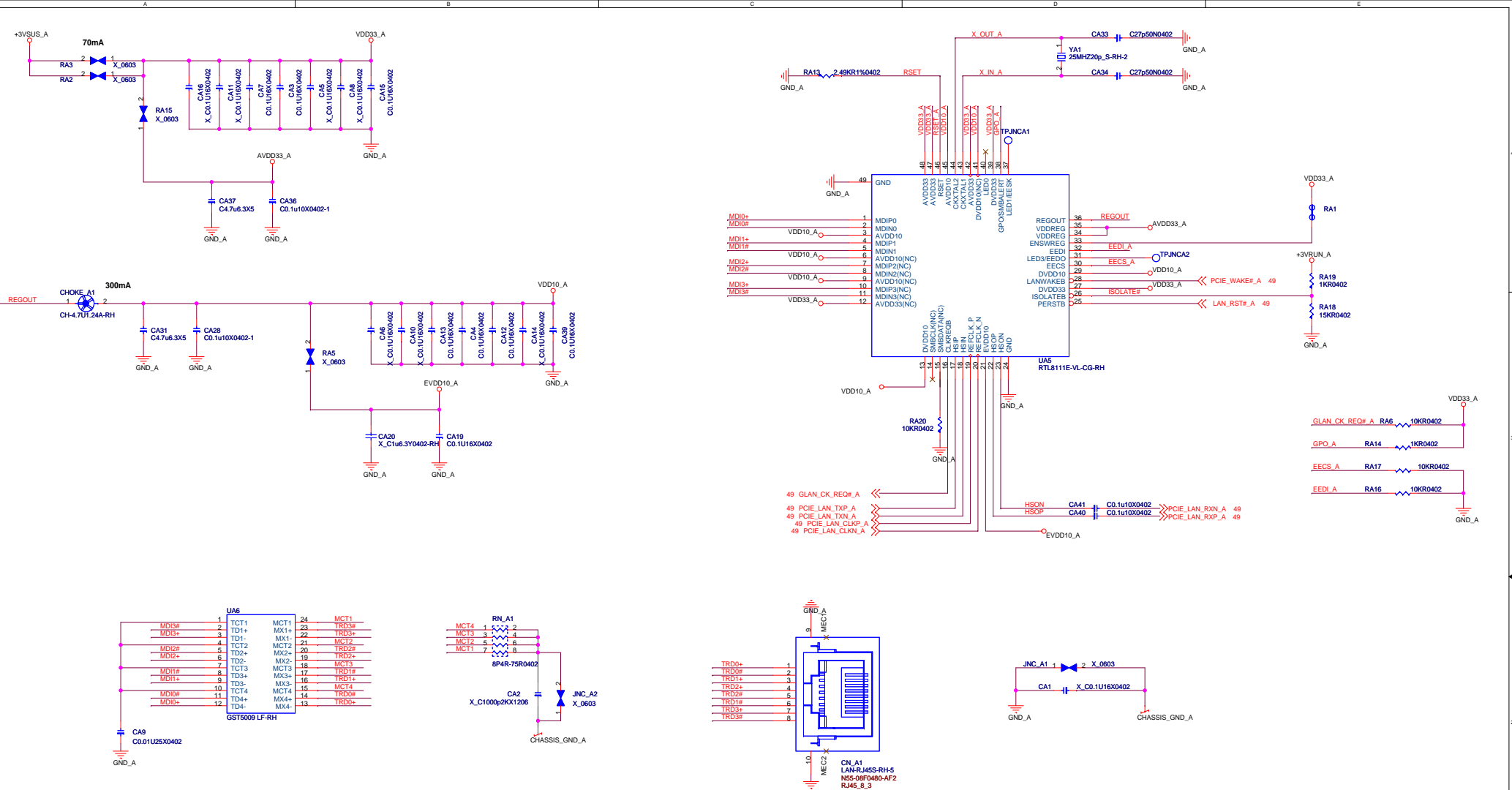


USB



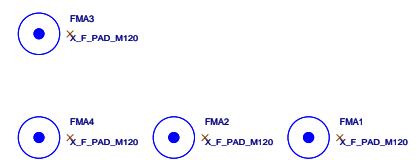
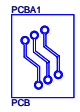
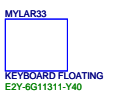
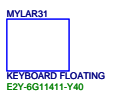
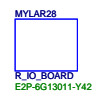
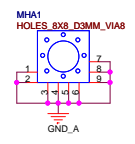
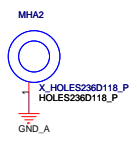
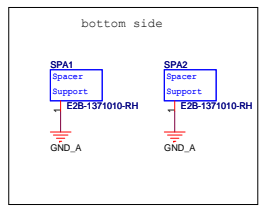
CRT



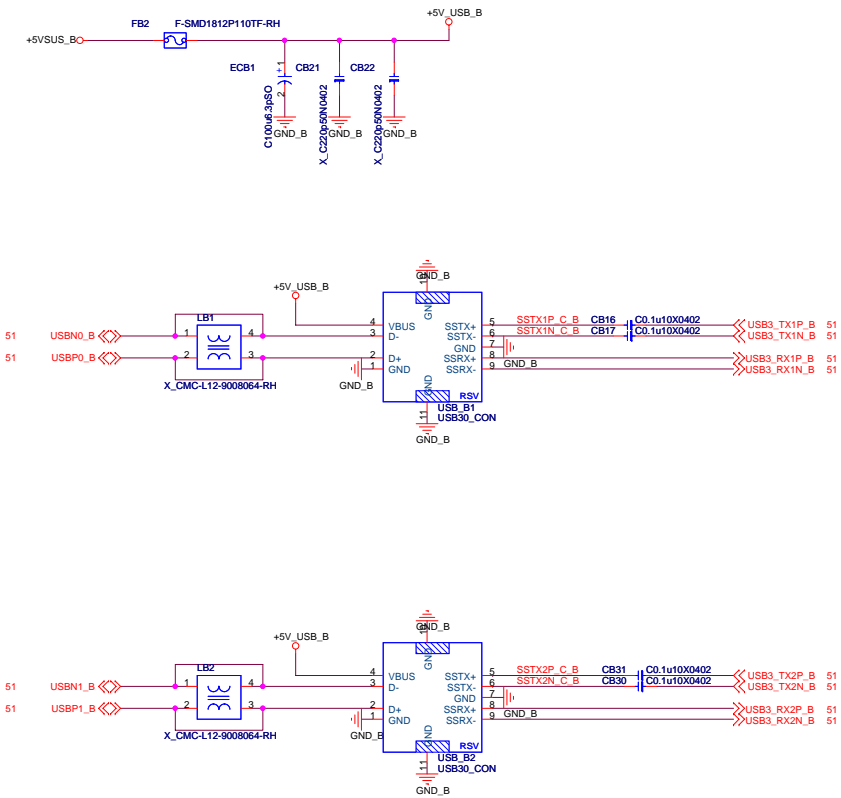


BTB STANDOFF

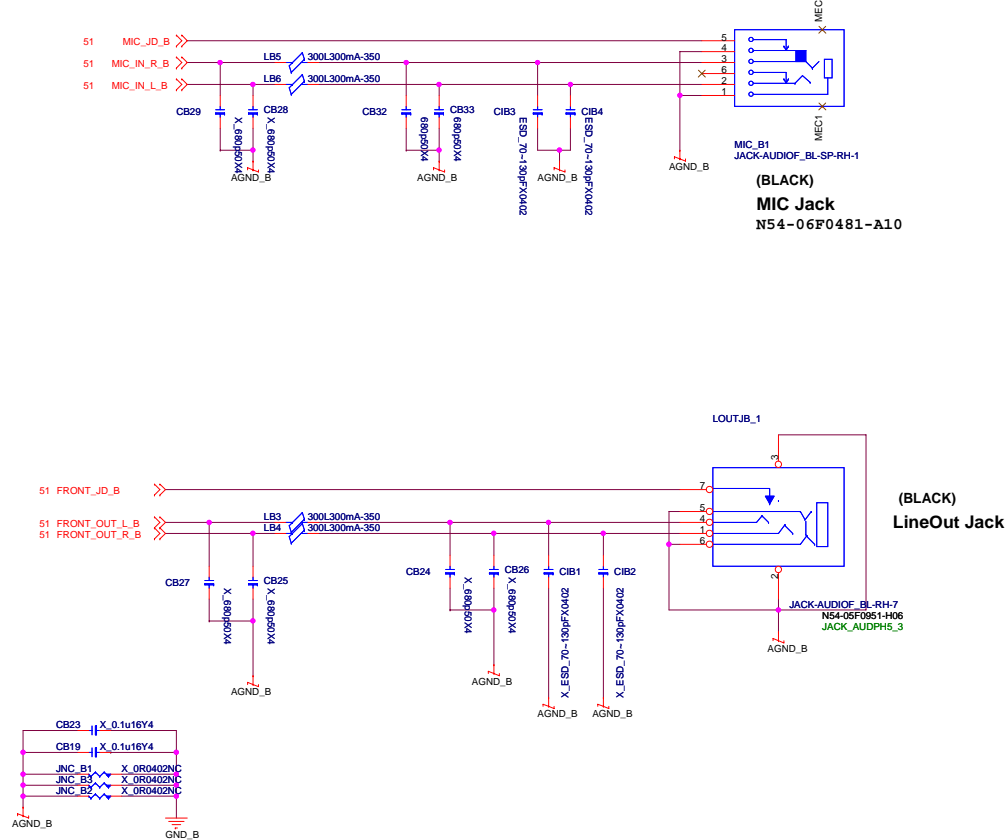
SCREW HOLE



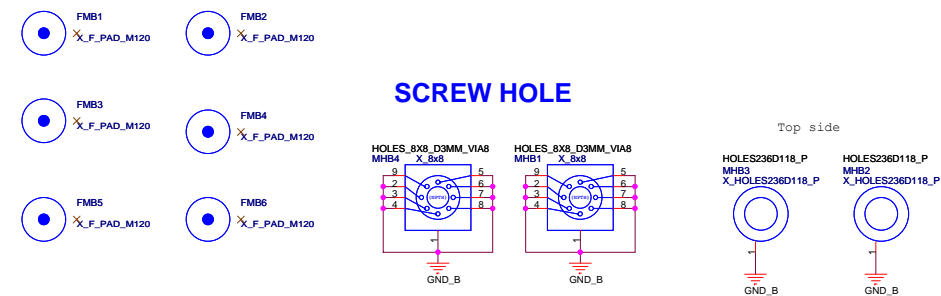
USB



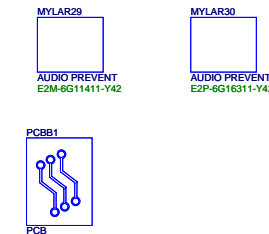
Audio Jack



SCREW HOLE



Audio Jack Mylar
for EMI suggestion



RC7 connection change from
+5VRUN_C to +5VSUS_C in 0B Ver .

